

Experimental Study of a Quadratic Boost: The Cascaded Connected Single Switch

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How to cite this paper: Honadia, P.A.A., Zouma, B., Ouédraogo, A. and Barro, F.I. (2024) Experimental Study of a Quadratic Boost: The Cascaded Connected Single Switch. *Smart Grid and Renewable Energy*, 15, 139-148.

<https://doi.org/10.4236/sgre.2024.156009>

Received: December 27, 2023

Accepted: June 25, 2024

Published: June 28, 2024

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Abstract

The quadratic boost is studied under its real model. The equations, of the continuous conduction mode, descriptive of this model are established. From these equations, the expressions of the voltage gain and the efficiency are extracted. These two quantities are plotted as a function of the duty cycle in order to appreciate them in different operating points of the transistor. The values of the different components have also been extracted for the fabrication of a prototype of the converter. Thanks to a set of experimental measurements at the input as well as at the output of the prototype converter, the voltage gain and the efficiency could also be observed. These were also plotted for different loads to observe converter behavior. The theoretical curves were compared with the experimental curves which allowed to validate the proposed mathematical models on a large range of duty cycles.

Keywords

Voltage Gain Factor, Conversion Efficiency, Duty Cycle, Quadratic Boost

1. Introduction

For practical reasons in the field of solar photovoltaic, photovoltaic inverters have managed to impose themselves naturally. Indeed a solar panel producing on average only 15 - 17 V, it would take several to get 250 - 300 V DC needed for 220 V AC in West Africa. In a will of miniaturization and minimization of the costs, the converters DC-DC elevators are used in the inverters to raise the tension of the panels. Most of these converters consist of passive and active switches

controlled by a pulse width modulator (PWM-Switch) [1]-[3]. A systematic method to obtain circuit-oriented average models for DC-DC converters was presented in the early 21st century [4]. Since then, many works have been done in the field with the aim of obtaining the best voltage gain and good efficiency for a suitable duty cycle [5]-[10]. Quadratic boost converters are among the structures that have been able to achieve most of these objectives. Several authors have tried to improve the performance of the quadratic boost converter by means of a structural change in its topology leading to new topologies with the same quadratic gain characteristic. The first one reported by Lascu *et al.*, was obtained by applying a rotation in the converter switching cells introducing a new converter in a power factor correction application [11]. Another one reported by Kadri *et al.*, was obtained by means of a software algorithm searching all the possible configuration with the same elements of the traditional basic quadratic boost allowing an application in photovoltaic conversion [12]. From these two topologies, it emerges mainly four boost converters of type quadratic type boost converters that are the Rotated Cell Single Switch (RCS2 - QB) and the Software Synthesized Single Switch (S4 - QB), as well as the Cascaded Connected Single Switch (C²S² - QB) and the Cascaded Connected Double Switch (C2DS - QB) [13]. However, they would be more interesting if the losses observed in the components could be minimized. To do this, we focused on the Cascaded Connected Single Switch (C²S² - QB) in order to highlight the losses observed using a mathematical model that we proposed. A prototype of the converter was then implemented, and its performance in terms of voltage gain and efficiency for different duty cycles were compared with those obtained by the proposed mathematical model. This will enable us to validate or reject our mathematical model.

2. Modeling, Mathematical Formulation and Application

2.1. Modeling, Mathematical Formulation

The real model of the quadratic boost, *i.e.* taking into account the losses in all components, is shown in **Figure 1**:

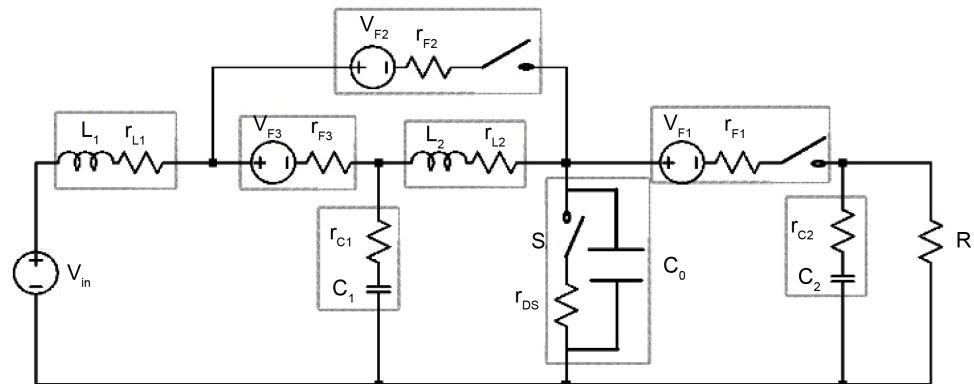


Figure 1. Quadratic boost with series losses and switching losses.

The power balance is written as:

$$P_I = P_0 + P_{LS} \quad (1)$$

With

$$P_{LS} = P_{r_L} + P_{r_C} + P_D + P_{FET} \quad (2)$$

P_b , P_o , P_{r_L} , P_{r_C} , P_D , P_{FET} are respectively the input power, the output power, the power losses through the inductors series resistance r_{L_1} , r_{L_2} , the power losses through the capacitors series resistance r_{C_1} , r_{C_2} , the power losses through the diode D_1 , D_2 , D_3 and, the power losses through the switch [14] [15].

Substituting each term by its expression, we obtain:

$$V_I * I_I = V_0 * I_0 + \left[\frac{r_{L_1} + \alpha(1-\alpha) \cdot r_{C_1}}{(1-\alpha)^4 \cdot R} + \frac{r_{L_2} + \alpha(1-\alpha) \cdot r_{C_2}}{(1-\alpha)^2 \cdot R} + \frac{R_F}{R} \left(\frac{1+(1-\alpha)^3}{(1-\alpha)^4} \right) + \frac{V_F}{V_0} \left(\frac{1+(1-\alpha)^2}{(1-\alpha)^2} \right) + \frac{r_{DS}\alpha}{(1-\alpha)^4 R} + \frac{1}{2} f_s C_0 R \right] \cdot \frac{V_0^2}{R} \quad (3)$$

From this expression, we can derive the gain in voltage:

$$G = \frac{V_0}{V_I} = \frac{(1-\alpha)^2 R}{(1-\alpha)^4 R + r_{L_1} + \left[\alpha(1-\alpha) \cdot r_{C_1} + (1-\alpha)^2 r_{L_2} + \alpha(1-\alpha)^3 \cdot r_{C_2} + R_F (1+(1-\alpha)^3) + \frac{V_F}{V_0} (1+(1-\alpha)^2) (1-\alpha)^2 R + r_{DS}\alpha + \frac{1}{2} f_s C_0 (1-\alpha)^4 R^2 \right]} \quad (4)$$

and the conversion efficiency:

$$\eta = \frac{P_0}{P_I} = \frac{P_0}{P_0 + P_{LS}} \quad (5)$$

$$\eta = \frac{1}{1 + \left[\frac{r_{L_1} + \alpha(1-\alpha) \cdot r_{C_1}}{(1-\alpha)^4 \cdot R} + \frac{r_{L_2} + \alpha(1-\alpha) \cdot r_{C_2}}{(1-\alpha)^2 \cdot R} + \frac{R_F}{R} \left(\frac{1+(1-\alpha)^3}{(1-\alpha)^4} \right) + \frac{V_F}{V_0} \left(\frac{1+(1-\alpha)^2}{(1-\alpha)^2} \right) + \frac{r_{DS}\alpha}{(1-\alpha)^4 R} + \frac{1}{2} f_s C_0 R \right]} \quad (6)$$

These different expressions were also used in the dimensioning for the making of the prototype.

2.2. Application

We went on the basis of an input voltage (voltage from the panels) of 12 V on average for an output voltage of 30 V. After the mathematical calculations to obtain the values of the components, the prototype has been realized as shown in **Figure 2**.

We make sure of the correct operation by visualizing the potential differences, as shown in **Figure 3**, at the terminals of the switches [14].

We have the control signal which is a square wave signal with a duty cycle of 0.36 that we have imposed on it. The transistor also receives the signal by the

shape of its gate voltage, which is similar to the PWM signal. The Drain-Source voltage signal is complementary to the Gate signal, so the transistor switches perfectly.

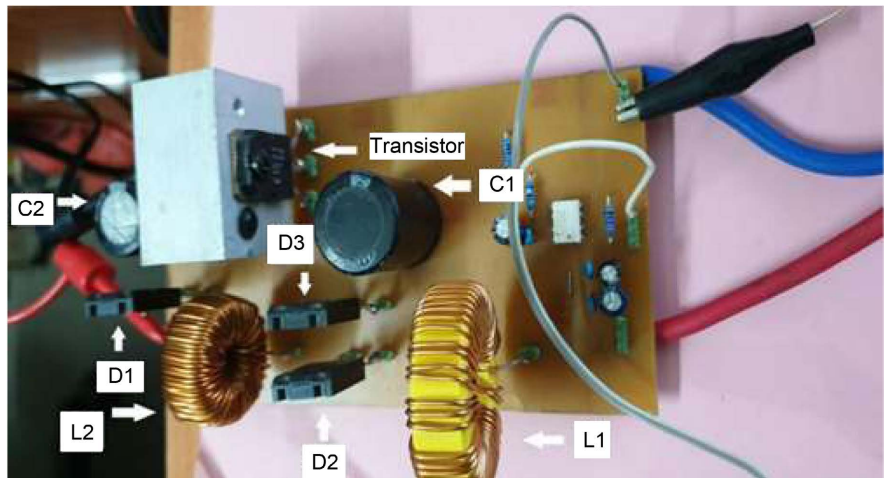


Figure 2. Prototype of quadratic boost.

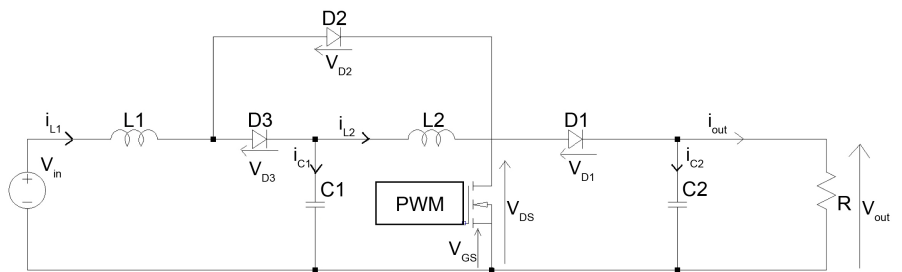


Figure 3. The different voltages visualized.

Also, we observe that the signal of V_{D2} signal is complementary to that of V_{DS} . It is therefore the same shape as the one of the Gate. The V_{D1} signal too is of the same shape as that of V_{DS} which is normal. It is therefore complementary like the signal of the voltage V_{D3} to that of the diode D_2 and the Gate as we expected.

We therefore observe the input and output voltages in **Figure 4**:

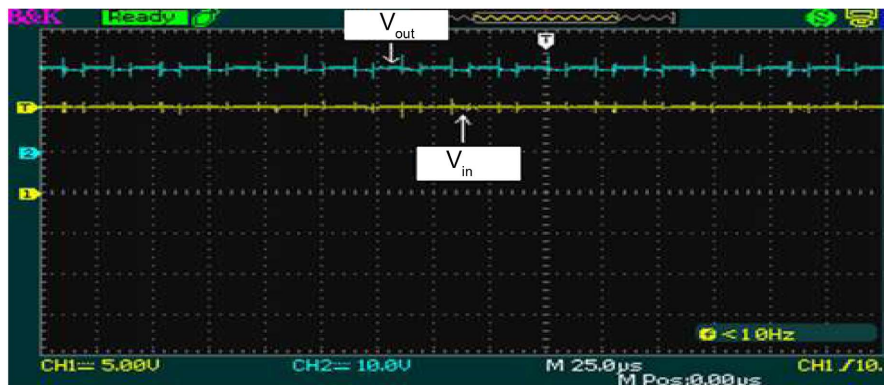


Figure 4. Oscillogram of the input and output voltages of the step-up quadratic.

These voltages seem correct in spite of the parasites observed on the output voltage. So we can therefore conclude that the device works perfectly.

3. Experimental Result and Discussion

Figure 5 and **Figure 6** show the ideal, theoretical curves including the real quadratic boost parameters and experimental curves for voltage gain factor and conversion efficiency. The ideal efficiency, which is unitary, has not been plotted.

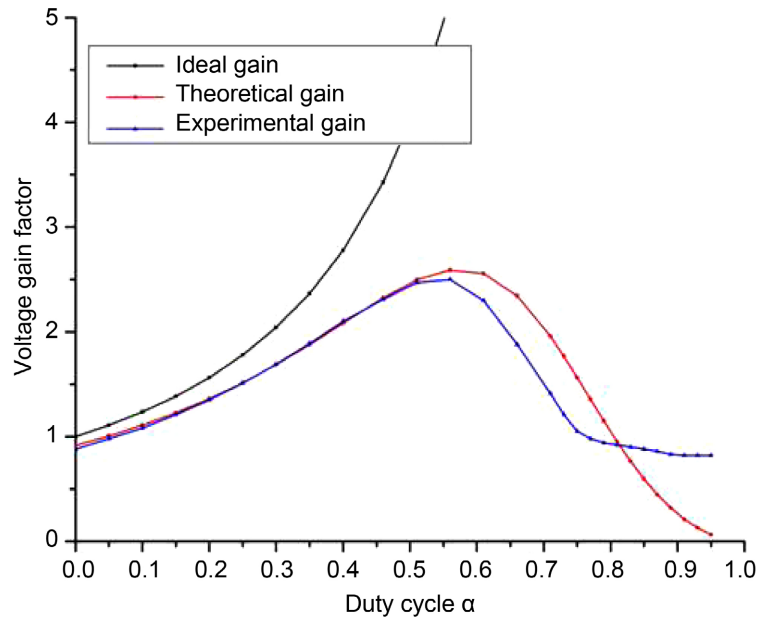


Figure 5. Comparison between the different voltage gains of the quadratic boost.

In **Figure 5**, the divergence from the ideal gain is quite noticeable even for low duty cycles. The losses recorded there are therefore quite considerable. Our model is quite faithful to the experimental gain up to a duty cycle of 0.5; beyond that, deviations are observed. Up to a duty cycle of 0.8, the error of the model could be explained by the evolution of the dynamic voltage of the diodes and the Drain-Source resistance of the transistor. Indeed, as seen above, the higher the duty cycle of the transistor is and the longer the switching time of the latter increases leading to an increasing power loss through the $r_{DS(on)}$ which also sees its value increase with temperature. However, this would not explain the phenomenon occurring for duty cycles greater than 0.8. This can also be seen in **Figure 6**, where the difference between the theoretical and experimental yields experimental yield is less than 10% until the cyclic ratio of 0.6 but being able to reach 30% beyond. The phenomenon reversing the tendency, for the cyclic ratios above 0.8, will be the subject of further study by us [14].

We now vary the operating point of the transistor by varying the load to observe the behavior of the converter.

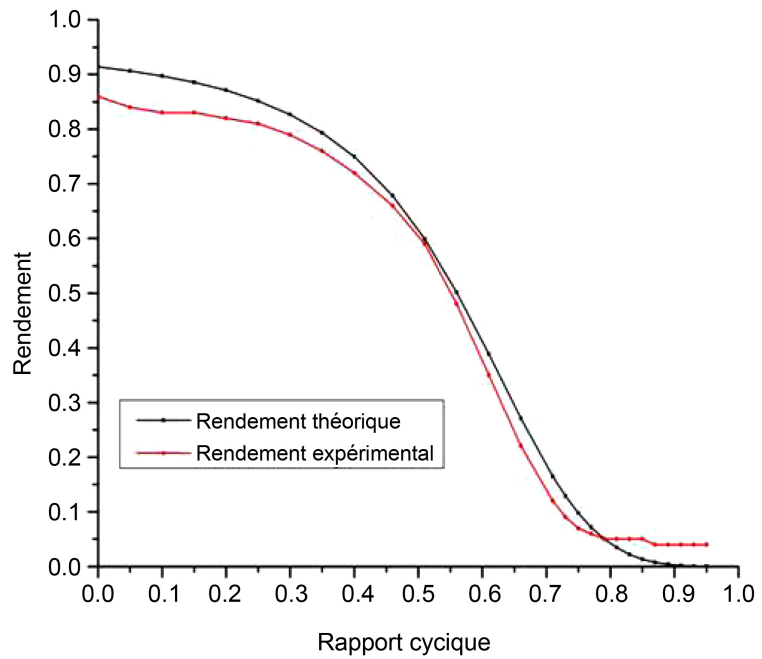
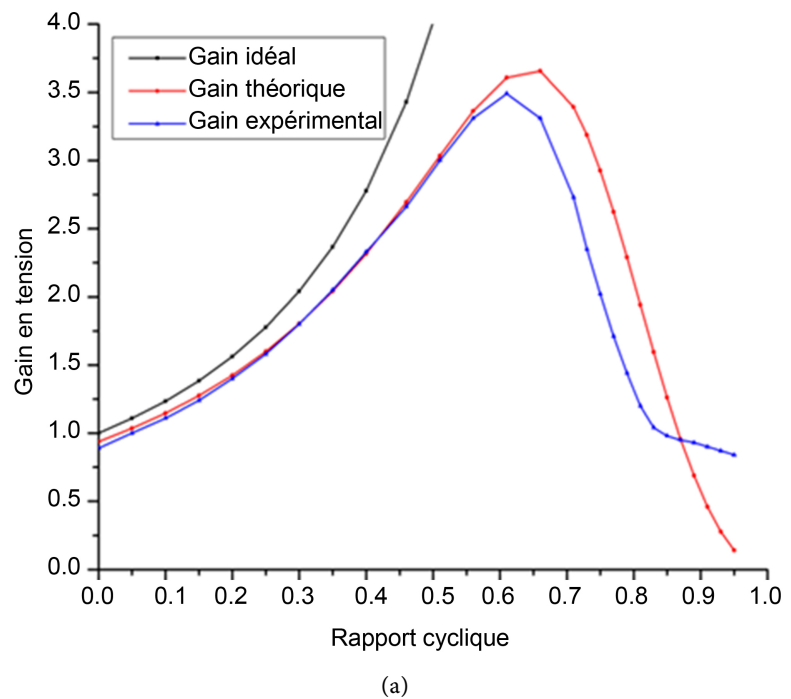
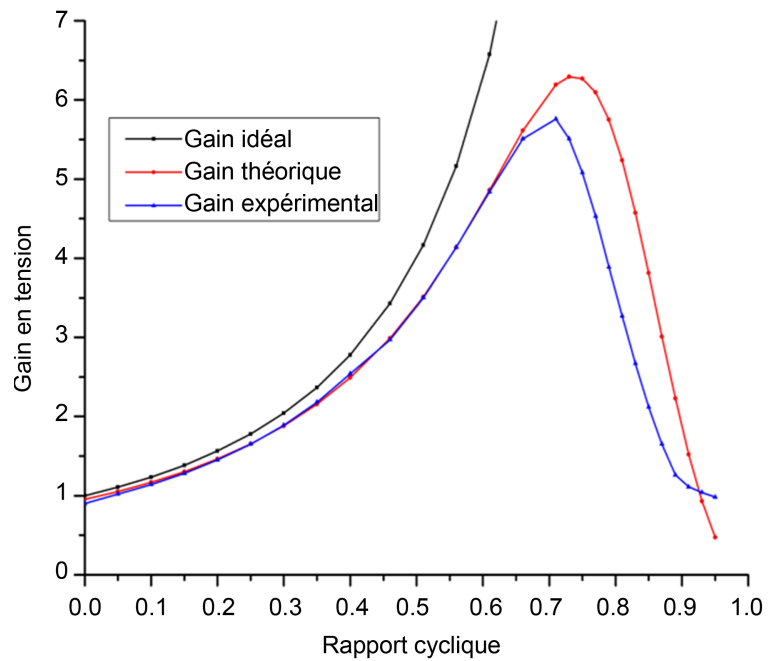


Figure 6. Comparison between the different conversion efficiency of the quadratic boost.

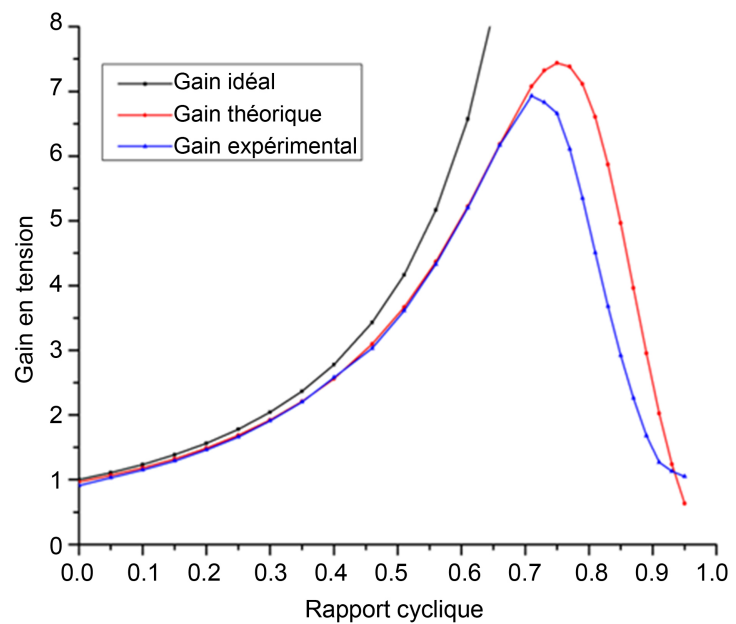
The curves in **Figure 7** show the voltage gains with resistors whose values are multiples of the initial resistance. We can see that our model always remains faithful to the experimental curve even if the deviations due to the temperature remain present for high duty cycles. Obviously, the higher the resistance, the better the gains., the better the gains are. In addition, the range of our unexplained phenomenon becomes narrower with this increase in resistance values.



(a)



(b)

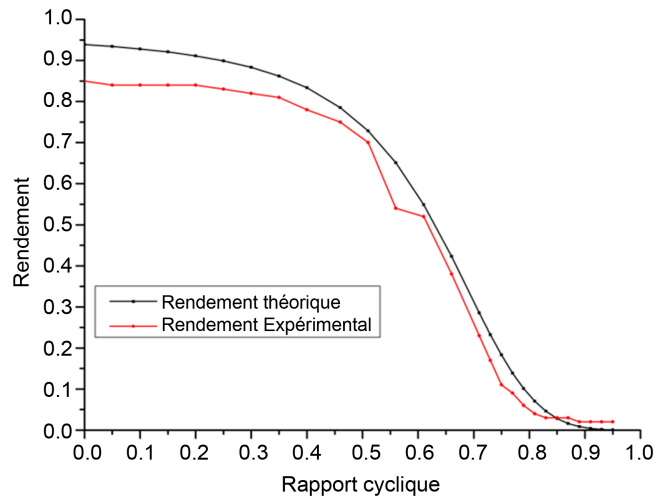


(c)

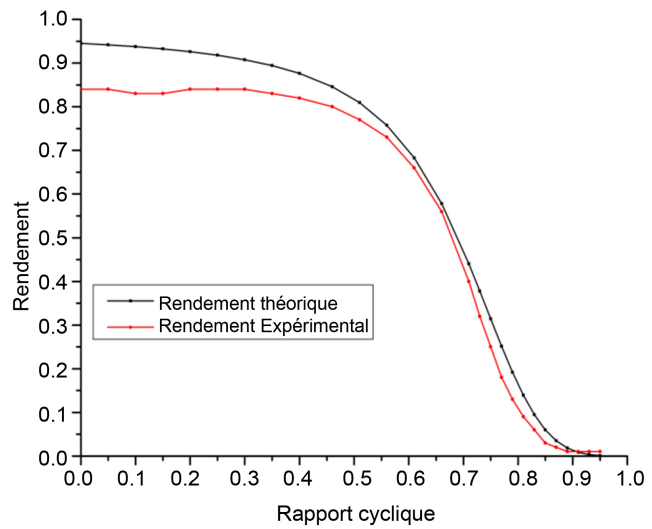
Figure 7. Voltage gain as a function of duty cycle for four different loads. (a) 47Ω ; (b) 141Ω . (c) 188Ω .

In **Figure 8**, the conversion efficiency curves will certainly tell us more.

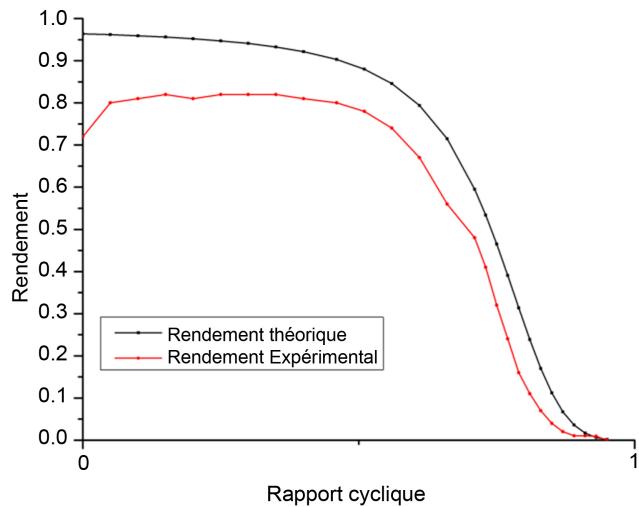
The efficiency evolves in the opposite way to the voltage gain as a function of the duty cycle, we observe less and less interesting efficiencies when we increase the value of the resistance. Nevertheless, our model remains sufficiently faithful to the experimental curves for low duty cycle values. Indeed, the deviations are always of the order of 10%. As observed previously with the gain curves, this is



(a)



(b)



(c)

Figure 8. Conversion efficiency as a function of duty cycle for four different loads. (a) 47 Ω; (b) 141 Ω. (c) 188 Ω.

related to the variations of our parameters with temperature that we did not integrate in the theoretical model with losses.

4. Conclusion

The set of measurements carried out on the prototype allowed us to draw the experimental curves of the converter performances, *i.e.* evolution of the gain and the conversion efficiency according to the duty cycle. These curves were compared with the theoretical curves obtained from our mathematical models. We were then able to observe that our models are satisfactory even for duty cycles of the order of 0.7. This difference between the theoretical model and the experimental data for duty cycles higher than about 0.7 - 0.8 is mainly due to the fact that our models do not take into account the evolution of the Drain-Source resistance r_{DSon} , the dynamic resistance of the diodes and their threshold voltages with temperature. This is not obvious as the law of evolution of the Drain-Source of the transistor with the temperature differs depending on the transistor all as the resistors dynamic of the diodes. In all the case, it remains not recommended operate with a ratio duty cycle greater than à 0.8 since this increases the stress on the diodes and the transistor and decreases thus the duration of life of the converter.

Acknowledgements

We would like to express our gratitude to ISP, University of Uppsala, Sweden, for its support of project BUF01.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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