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Electrostatic Coupling and Threshold Engineering in Low-Temperature µc-Si Double-Gate TFTs

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Abstract

Thin-film electronics based on microcrystalline silicon (µc-Si) is today a key platform for flexible and low-temperature applications. In this context, the double-gate architecture provides an additional electrostatic degree of freedom that enables fine tuning of the key parameters of TFTs. This work presents a comprehensive experimental and numerical study of electrostatic coupling between gates in low-temperature-processed µc-Si double-gate TFTs. The investigated devices consist of an undoped µc-Si active layer of either 30 nm or 200 nm thickness deposited by PECVD, with a bottom gate insulated by Si_3N_4 and a top gate insulated by RF-sputtered SiO_2. Electrical measurements show that, for thin films, the threshold voltage varies almost linearly with the top-gate bias, revealing a strong inter-interface coupling. In contrast, thick films exhibit almost no threshold modulation, due to significant volumetric screening. Moreover, a back-channel formation is observed under positive top-gate bias, consistent with mechanisms reported in the literature for multi-interface architectures. A complete numerical model was developed in SILVACO ATLAS to interpret these phenomena. The model incorporates a detailed description of µc-Si based on four exponential distributions representing band-tail states and deep defect states, in accordance with models derived for amorphous silicon. The simulations accurately reproduce the experimental curves and confirm that the penetration of the electric field from both gates through the active layer is only effective at low thickness. They also reveal that the appearance of the second channel results from electron accumulation induced by the back-gate bias. This study highlights the decisive role of active-layer thickness and defect density in the operation of µc-Si double-gate TFTs. The results open promising perspectives for the optimization of devices re-

quiring enhanced electrostatic control, including flexible circuits, large-area sensors, and low-power electronics.

Keywords

Microcrystalline Silicon, Double-Gate TFT, Threshold Voltage Modulation, Band-Tail and Deep States, SILVACO ATLAS Simulation

1. Introduction

Flexible large-area electronics have expanded rapidly due to thin-film transistors (TFTs) that can be processed at low temperature. Early demonstrations of polysilicon circuits on flexible metal foils confirmed the feasibility of robust portable systems [1]. Following this trend, microcrystalline-silicon (μc-Si) TFTs have attracted interest due to their mechanical robustness, decent mobility, and compatibility with low-temperature PECVD processes [2].

However, μc-Si presents a granular microstructure that generates a high density of deep states, causing mobility degradation, Vth instability and poor subthreshold swing, as established by classical defect-state models [3]. Several architectural advances have been proposed, including ultra-thin-channel structures inspired by FinFETs [4], while early studies on polysilicon TFTs highlighted the importance of transverse-field control [5]. Experimental work on μc-Si TFTs demonstrated that thinning the active layer enhances threshold modulation and produces SOI-FET-like behavior [6] [7], while insights into flat-panel display architectures refined the understanding of electrostatic coupling [8].

The double-gate (DG) architecture represents a key evolution to further improve channel control. Recent studies in oxide, organic and hybrid TFTs demonstrated enhanced transport [9], improved subthreshold performance [10], stronger modulation in ultra-thin channels [11], efficient back-channel control [12] [13], and improved stability under electrical stress [14].

Yet, few works combine μc-Si double-gate experiments, full ATLAS modeling including band-tail and deep states, and a systematic comparison between thin and thick films. This work addresses this gap by investigating:

1) the fabrication and characterization of μc-Si DG-TFTs,

2) linear Vth modulation and possible back-channel formation,

3) an ATLAS model including full DOS representation,

4) the impact of active-layer thickness on inter-interface coupling.

This study builds upon classical μc-Si/SOI TFT work [1]-[8] and modern multi-gate TFT physics [9]-[19].

2. Experimental Methodology

2.1. Device Structure and Fabrication Process

The thin-film transistors investigated in this work use an independent double-

gate architecture designed to enable simultaneous electrostatic control from both channel interfaces. This approach follows the pioneering studies on low-temperature μc-Si TFTs for flexible electronics [2] and on ultra-thin active layers in structures analogous to SOI-FETs [6] [7].

The general device structure is shown in **Figure 1**. The undoped microcrystalline-silicon (μc-Si) active layer is deposited by PECVD under very low-temperature conditions to ensure compatibility with thermally sensitive substrates, as demonstrated in [2] and in more recent analyses of flexible-electronics TFTs [11] [16]. The active-layer thickness of 50 nm is selected to enhance sensitivity to the transverse electric fields generated by both gates, consistent with earlier studies on thin μc-Si layers [6] [7].

On the experimental side, the characteristics used in this work originate from previously fabricated and characterized μc-Si devices with a 50-nm active-layer thickness. In the simulation part, we selected a 30-nm thickness, a value identified in earlier studies on single-gate TFTs as particularly favorable for electrostatic control. This optimized geometry was then adapted to the double-gate architecture investigated in this work.

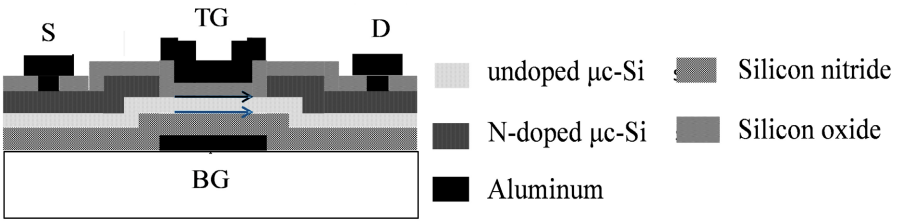

Figure 1. Structure of the double-gate TFT with the top gate (TG) and the bottom gate (BG).

The bottom gate (BG) is separated from the channel by a 300-nm Si_3N_4 layer, a dielectric commonly used in conventional μc-Si TFTs for its favourable electrical properties [2]. The top gate (TG) is isolated from the channel by a 160-nm SiO_2 layer deposited by RF sputtering without heating, a process well-suited to low-temperature and flexible technologies [1] [2] [11].

Source and drain electrodes are designed to ensure ohmic contacts, which is essential to guarantee that the observed behaviours arise solely from channel and interface effects, rather than contact limitations.

This structural configuration enables isolated and precise investigation of the electrostatic effects induced by the second gate. It is consistent with modern double-gate designs in metal-oxide, organic, and hybrid TFTs, such as those reported in [9]-[11].

Experimentally, the transfer characteristics used in this work come from previously fabricated μc-Si TFTs with a 50-nm active layer. In the simulation study, a 30-nm active layer was selected because earlier studies on single-gate μc-Si TFTs had already demonstrated that this thickness provides the best electrostatic control. This optimized geometry was then adapted to the double-gate architecture investigated here, while the 200-nm case was included as a comparison to illus-

trate volumetric screening in thick films.

2.2. Electrical Measurement Protocol

Electrical measurements were carried out under static conditions to extract the transfer characteristics of the device as a function of the top-gate bias. Specifically, $I_{DS} - V_{GBG}$ curves were recorded at a fixed drain–source voltage $V_{DS} = 1\,\text{V}$, while the applied top-gate voltage V_{TG} was swept between −15 V and +15 V.

This methodology, typical of studies focusing on multi-interface phenomena [5] [12] [14], allows:

- evaluation of the direct influence of the top gate on channel formation,
- identification of possible threshold-voltage modulation,
- detection of back-channel phenomena, extensively studied in modern double-gate architectures [11] [13] [15].

Figure 2 shows the drain current I_{DS} transfer characteristics as a function of the bottom-gate voltage for different fixed values of the top-gate voltage, measured at a drain-source voltage of +1 V.

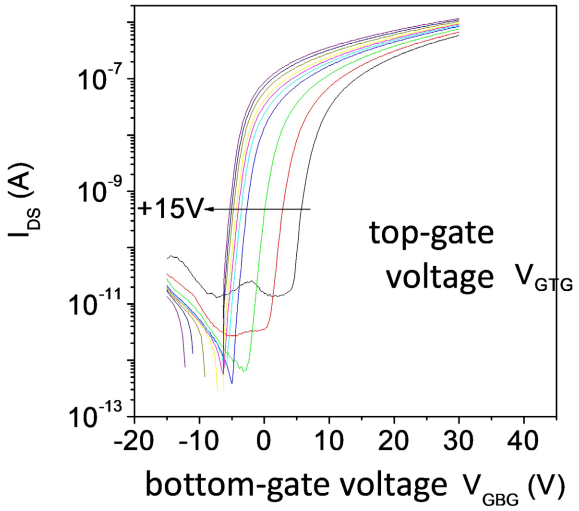

Figure 2. Drain current IDS transfer characteristic as a function of the bottom-gate voltage for different fixed values of the top-gate voltage, measured at a drain-source voltage of +1 V.

As observed in **Figure 2**, the experimental results show a pronounced and nearly linear shift of the transfer curves under the effect of V_{TG}, indicating strong electrostatic coupling between the two interfaces. This behaviour is particularly prominent in thin films and has also been reported in modern multi-gate TFTs based on organic and oxide semiconductors [10]-[13].

2.3. Threshold-Voltage Extraction and Analysis of Its Variation

The main parameters extracted from the experimental characteristics include:

- the threshold voltage V_{th}, determined either by linear-region extrapolation or

through classical methods reported in the literature [3] [7];

- the subthreshold slope (S), an indicator of the electrostatic quality of the channel;
- the off-state current (I_{off}), which is sensitive to deep states and back-channel effects;
- the variation ΔV_{th} (V_{TG}), used to directly quantify inter-interface coupling.

The variation of the threshold voltage as a function of the top-gate bias is shown in **Figure 3**.

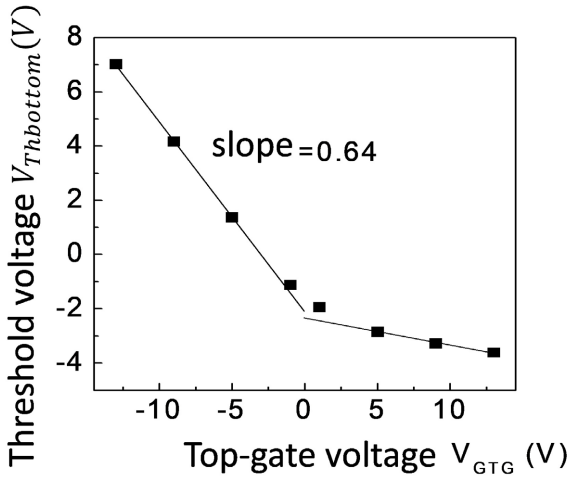

Figure 3. Shift of the threshold voltage, extracted from the I_{DS} -bottom-gate voltage (V_{GBG}) transfer characteristic, as a function of the top-gate voltage (V_{TG}).

The threshold-voltage variation extracted from the transfer curves (**Figure 3**) shows that V_{th} evolves quasi-linearly with the top-gate voltage. This trend, also reported in recent technologies such as double-gate IGZO TFTs [9] [12], reflects a highly efficient electrostatic coupling between the two channel interfaces. The steep slope observed for negative V_{TG} confirms that the electric field applied by the top gate directly influences channel formation, even in a granular material such as µc-Si.

When VTG becomes strongly positive, the dependence of Vth slightly decreases. This behaviour is attributed to the formation of an accumulation region at the upper interface, which reduces the sensitivity of the channel to the field originating from the bottom gate, consistent with accumulation/depletion effects reported in [2] [5] [14]. In parallel, variations in SS and I_{off} are observed, consistent with the emergence of a back channel under positive top-gate bias, a phenomenon widely discussed in [13] [14] [16].

These observations demonstrate that the very small active-layer thickness enables a direct interaction between the two gates, similar to that observed in ultra-thin SOI FinFETs. The geometric proximity of the interfaces mitigates the impact of bulk trapping, allowing the electric field to extend across the entire channel thickness. These findings form the physical foundation of the SILVACO model-

ling presented in the next section.

3. SILVACO Numerical Modeling of Double-Gate TFTs

3.1. Physical Model of the Microcrystalline Silicon Material

The active layer of the TFTs studied in this work is microcrystalline silicon (μc-Si), whose microstructure consists of nanometric grains (<50 nm) separated by grain boundaries containing a high density of electrically active defects. Considering the dimensions of the channel (L = 20 μm, W = 100 μm), the number of grains is sufficiently large to allow a statistical treatment of their effects. Thus, the active layer is modelled as a homogeneous material containing a uniform distribution of defects. This homogeneous representation averages grain-boundary effects. While more advanced models may explicitly resolve individual grains, the adopted approach offers an accurate large-area statistical description compatible with the device dimensions considered.

Based on classical models for disordered semiconductors [4] [17] the defect density of states (DOS) in the bandgap of μc-Si can be described by four exponential functions, replacing the Gaussian distributions often used for amorphous silicon [6] [18]:

Band-tail states

$$g_{TA}(E) = N_{TA} \exp\left[\frac{E - E_C}{W_{TA}}\right] \tag{1}$$

$$g_{TD}(E) = N_{TD} \exp\left[\frac{E_V - E}{W_{TD}}\right] \tag{2}$$

Deep states

$$g_{GA}(E) = N_{GA} \exp\left[\frac{E - E_c}{W_{TA}}\right] \tag{3}$$

$$g_{GD}(E) = N_{GD} \exp\left[\frac{E_V - E}{W_{TD}}\right] \tag{4}$$

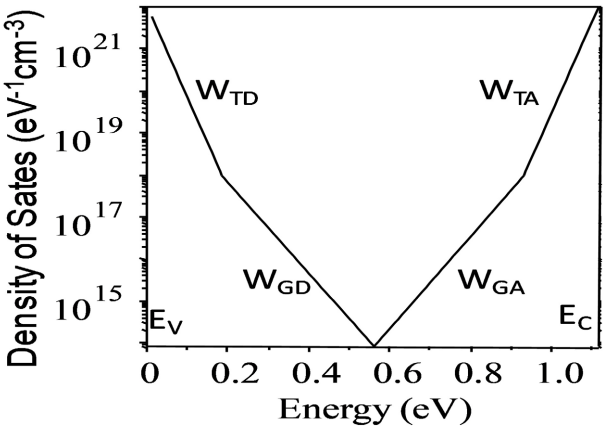

Figure 4. Distribution of the density of states within the silicon bandgap [4] [5] [17].

These four exponentials, illustrated in **Figure 4** [4] [5] [17] represent:

- the conduction-band tail (g_{TA}),
- the valence-band tail (g_{TD}),
- the deep states near the conduction side (g_{GA}),
- the deep states near the valence side (g_{GD}).

Experimental validation of the model: central role of Figure 5

To validate the DOS model, transfer characteristics of N-type and P-type TFTs fabricated simultaneously on the same 100-nm undoped µc-Si active layer (**Figure 5(a)**) were analyzed using the incremental method introduced in [6] [18]. These devices are ideal for validation because:

1) both TFTs share the same microstructure and defect distribution,

2) N and P conduction probe different sides of the bandgap,

3) the transconductance directly reflects the kinetics of the Fermi level as it sweeps through the DOS.

The extracted DOS profile (**Figure 5(b)**) exhibits a continuous distribution around mid-gap that fits remarkably well with the four-exponential model, confirming its physical relevance and consistency with previous microcrystalline-silicon studies [4] [5] [7] [17].

Figure 5 is therefore essential, as it provides experimental evidence supporting the DOS model used in the simulation.

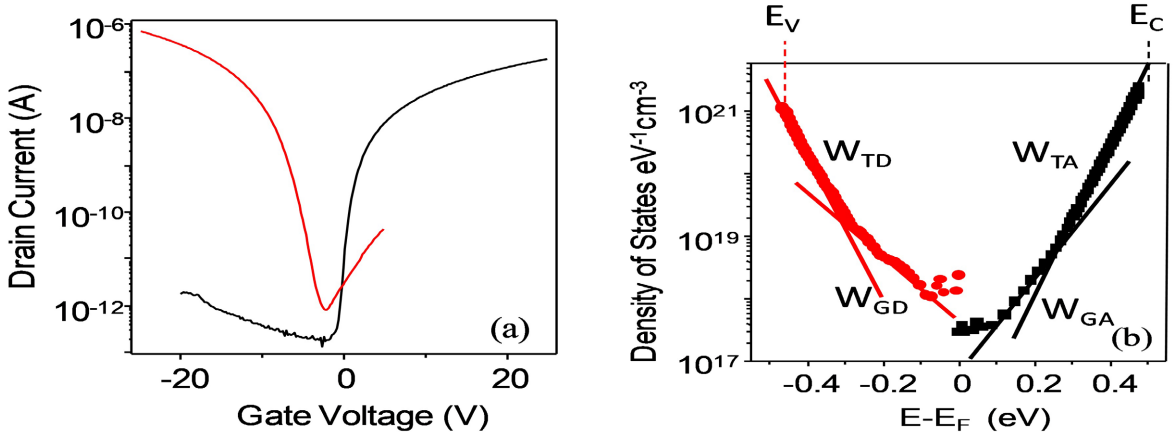

Figure 5. Density of states inside the bandgap of a microcrystalline-silicon film (b), extracted from the transfer characteristics (a) [8] of N-type and P-type TFTs fabricated simultaneously on a 100-nm-thick undoped µc-Si layer.

The N-type TFT has a channel length L = 20 µm and width W = 20 µm, while the P-type TFT has a channel length and width of 20 µm and 80 µm, respectively.

3.2. Construction of the Simulated Structure (ATHENA/ATLAS)

The simulated structure (**Figure 6**) faithfully reproduces the experimental devices:

- Si substrate: 700 µm,
- Undoped µc-Si active layer: 30 nm or 200 nm,
- N^+ doped µc-Si: 70 nm (10^{19} cm^{-3}),

- Bottom dielectric: Si_3N_4 (150 - 300 nm),
- Top dielectric: SiO_2 (160 nm, RF sputtered without heating),
- Architecture: independent double-gate.

A refined vertical mesh (1 nm) is used to accurately capture:

- front-channel formation,
- possible back-channel formation,
- potential and charge-distribution gradients.

All layer depositions and etches are defined in ATHENA, while transport equations are solved in ATLAS.

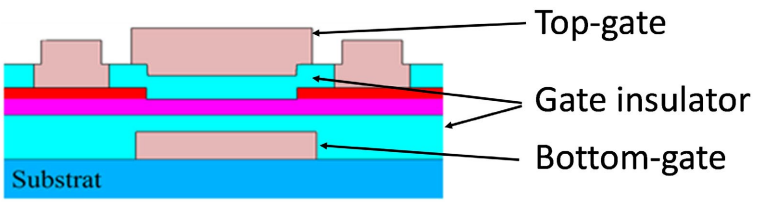

Figure 6. Simulated structure of the double-gate thin-film transistors (TFTs).

3.3. Simulation: Influence of the Second Gate (Thin Film, 30 nm)

Figure 7(a) and Figure 7(b) show the transfer characteristics of a 30-nm µc-Si TFT:

- without defects (ideal case),
- with defects using $W_{TA} = 22\,\text{meV}$ and $W_{GA} = 41\,\text{meV}$.

When the second gate is biased from −7 V to +7 V, a clear quasi-linear shift of the curves is observed, confirming the experimental trends (**Figure 8**). The threshold-voltage modulation is:

- much stronger in the defect-free film,
- reduced in the presence of deep states, due to electrostatic screening.

Back-channel formation

In the defective case (Figure 7(b)), shoulders appear at $V_{TG} = +3\,\text{V}$ and $+7\,\text{V}$, indicating:

- electron accumulation at the back interface,
- formation of a secondary conduction channel,
- an apparent (but artificial) reduction of V_{th}.

The behavior observed in Figure 7 is also consistent with the well-documented effect of ultra-thin channel layers improving electrostatic control in µc-Si TFTs [5] [8] [19], as previously reported in thin-film devices with strong interface coupling.

The back-channel formation mechanism (Figure 9), typical of poorly passivated µc-Si TFTs, also aligns with earlier analyses presented in [8] [19], where fixed positive charges at the rear interface induce a secondary conduction path.

After back-channel correction, the resulting V_{th} (V_{TG}) curve (Figure 10) closely matches experimental behavior.

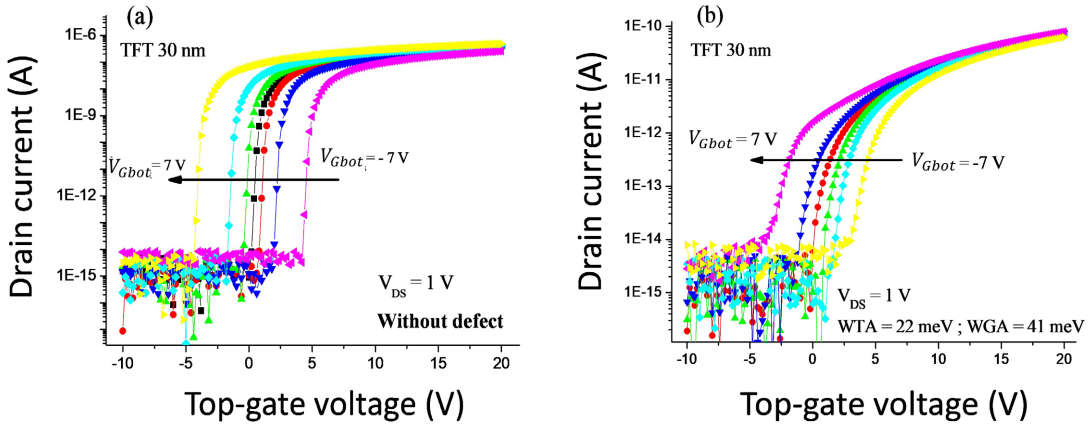

Figure 7. Semi-logarithmic transfer characteristics of a TFT (a) without defects and (b) with a defect density in the silicon layer, obtained for different values of the secondary-gate voltage.

Threshold-voltage evolution and comparison between defect-free and defective films

Figure 8 presents the evolution of the threshold voltage as a function of the second-gate voltage for both TFTs (with and without defects).

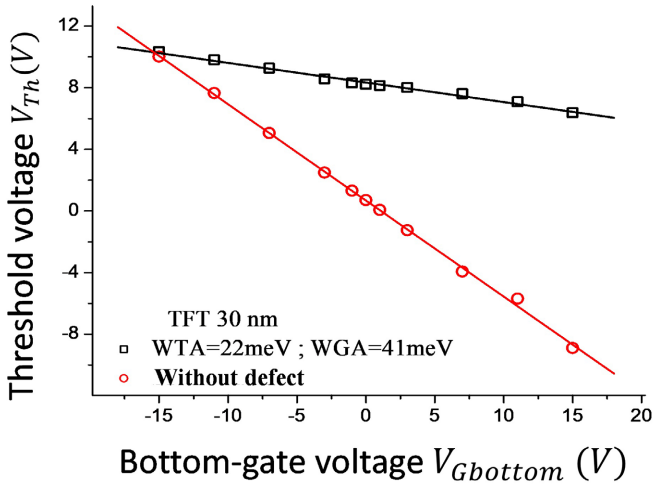

Figure 8. Threshold voltage as a function of the secondary gate voltage for TFTs with and without defects in the silicon layer.

From **Figure 8**, several points become clear:

1) V_{th} varies linearly with V_{TG} regardless of the defect density in the silicon layer.

2) The slope of V_{th} (V_{TG}) is significantly larger in defect-free films, reflecting a stronger front/back coupling.

3) Experimental curves show two distinct slopes, corresponding to negative and positive gate biases.

This dual-slope behavior originates from back-channel formation, as described

below.

Back-channel formation

As shown in Figure 7(b), for $V_{TG} = +3\,\text{V}$; and $+7\,\text{V}$, the transfer curves exhibit "shoulders", characteristic of a secondary channel forming at the back interface when the main gate is biased negatively.

This phenomenon is well known in μc-Si TFTs and is illustrated in the experimental Figure 9, which reports:

- a bottom-gate TFT with a strong back-channel effect (two rises in I_{DS}),
- a top-gate TFT where the back channel appears only as a shoulder.

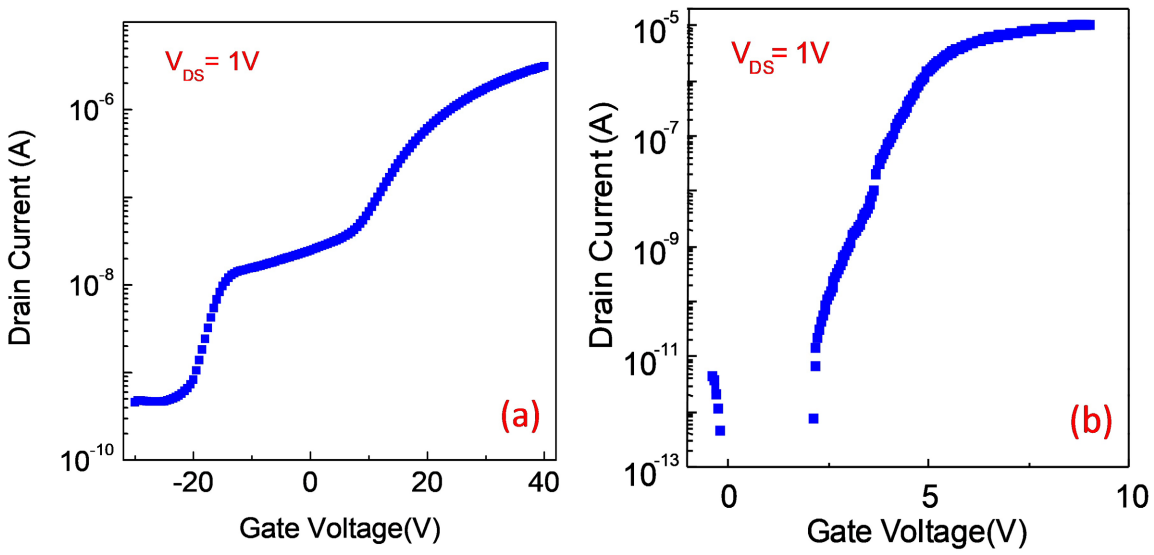

Figure 9. Experimental μc-Si TFT transfer curves showing strong back-channel effects [8]. (a) poorly passivated bottom-gate TFT; (b) top-gate TFT with fixed positive charges at the back interface.

In both cases, positive fixed charges at the back interface generate electron accumulation, producing a secondary conduction path.

In this context, a "poorly passivated" interface refers to a high density of interface traps or fixed positive charges that locally accumulate electrons. In our simulations, the observed back-channel does not arise from artificially introduced fixed charges but from field-induced accumulation caused by the secondary-gate bias, consistent with the defect distribution used.

In our double-gate TFTs

Back-channel formation occurs when the rear gate is positively biased ($+3\,\text{V}$, $+7\,\text{V}$).

When this happens:

- a second channel forms at the bottom interface,
- the apparent threshold voltage decreases artificially,
- the V_{th} (V_{TG}) curve deviates from linearity.

This is why Figure 10, which corrects the back-channel contribution, yields a threshold-voltage trend much closer to the experimental measurements.

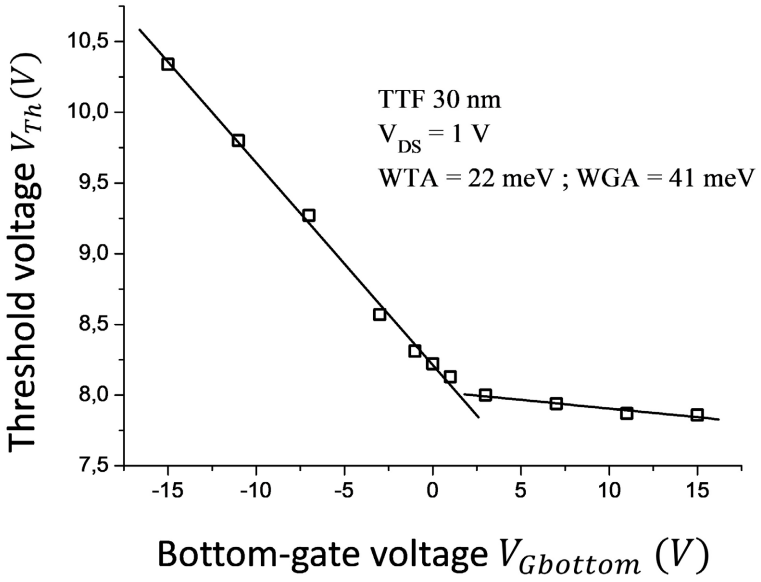

Figure 10. Corrected threshold voltage for a 30-nm TFT with defects ($W_{TA} = 22\,\text{meV}$; $W_{GA} = 41\,\text{meV}$).

Comparison with thicker devices (200 nm)

As shown previously in the literature, thicker µc-Si layers tend to screen electric fields and prevent dual-gate coupling [2] [4] [19], which explains the absence of threshold modulation in **Figure 11**.

To further analyze the influence of film thickness, a second double-gate TFT with a 200 nm active layer and identical defect parameters was simulated. The corresponding transfer curves for various V_{TG} values ($-7\,\text{V}$ to $+7\,\text{V}$) are shown in **Figure 11**.

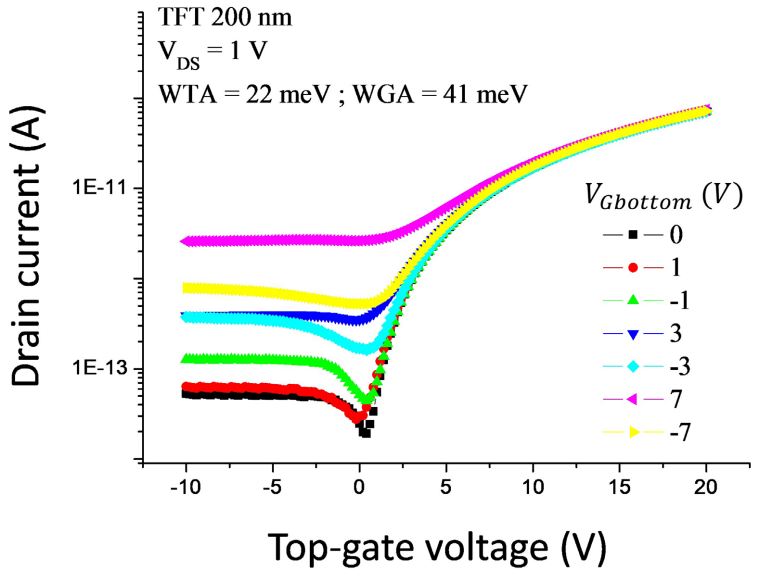

Figure 11. Transfer characteristics of a 200-nm µc-Si double-gate TFT under various secondary-gate voltages.

The main result is unambiguous:

- no threshold-voltage shift occurs,
- the subthreshold swing degrades,
- the off-state current increases with $|V_{TG}|$.

This behavior confirms that thicker μc-Si layers screen the electric field of the second gate, suppressing inter-interface coupling.

4. Conclusions

This study has demonstrated, through a combined experimental and numerical approach, the decisive influence of the second gate on the operation of microcrystalline-silicon thin-film transistors. The results show that the double-gate architecture enables a dynamic and nearly linear modulation of the threshold voltage, particularly effective in thin films where the electric field fully penetrates the active layer. This confirms that low-thickness devices exhibit enhanced inter-interface coupling, similar to what is observed in advanced SOI and FinFET structures.

The SILVACO ATLAS simulations accurately reproduced the experimental behavior, validating the defect-density model based on four exponential functions to represent band-tail states and deep defects. They also reveal the formation of a back-channel in thin layers under positive bias of the secondary gate, whereas thicker films remain insensitive to this modulation due to volumetric screening.

Overall, this work highlights the key role of active-layer thickness and defect density in engineering μc-Si double-gate TFTs. The results pave the way for optimizing such structures for flexible electronics, low-power circuits, and devices requiring advanced electrostatic control. Such tunable Vth behavior is highly desirable in flexible and low-power circuits, as it enables compensation for process variability, multi-Vth design on the same substrate, and adaptive biasing strategies essential for low-leakage and sensor-interface circuitry.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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Abbreviations

AL: Active layer
BG: Bottom gate
DG-TFT: Double-gate thin-film transistor
GD: Gate dielectric/Gate insulator
I_D: Drain current
MG: Main gate
μc-Si: Microcrystalline silicon
PECVD: Plasma-enhanced chemical vapor deposition
RF: Radio frequency (RF sputtering)
SG: Secondary gate
Si: Silicon
Si_3N_4: Silicon nitride
SiO_2: Silicon dioxide
SiO_X: Silicon oxide
TFT: Thin-film transistor
TG: Top gate
V_{BG}: Bottom-gate voltage
V_D: Drain voltage
V_{TG}: Top-gate voltage
V_{th} (or V_t): Threshold voltage