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Design & Analysis of 5 nm PDSOI and FDSOI n-MOSFETs for Ultra-Low Power Applications with High-k Dielectric Materials

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Abstract

In this study, a comparison of 5 nm PDSOI and FDSOI n-MOSFETs with SiO_2 and high-k gate dielectrics is carried out using Silvaco TCAD ATLAS platform with necessary models. SOI architectures (PDSOI/FDSOI) offer enhanced electrostatic control compared to bulk CMOS, which suffers from threshold instability, SCEs and leakage near the 20 nm node. In this scaling, various high-k dielectric materials were explored for gate oxide. Among those, Ta_2O_5 shows comparatively much better results with respect to the optimized SiO_2-gated device of the same SOI architecture. The PDSOI device showed 39.15% lower Threshold Voltage (V_{th}), 26.5% improved Subthreshold-Swing (SS), leakage current (I_{OFF}) of 2.17×10^{-10} A, and I_{ON}/I_{OFF} ratio of 1.64×10^6, making it suitable for analog and near-threshold logic applications. The FDSOI device exhibited closely unchanged V_{th} of 0.6604 V, 34% improved SS, ultra-low I_{OFF} of 1.69×10^{-13} A and I_{ON}/I_{OFF} ratio 7.41×10^9 favoring use in high-speed and ultra-low-leakage digital systems. This paper gives valuable insight and guidelines for selecting optimal SOI architectures and gate dielectric materials in future ultra-scaled, energy-efficient, and high-performance integrated circuits.

Keywords

PDSOI, FDSOI, 5 nm Node, High-k Gate Dielectric, n-MOSFET

1. Introduction

The ever-increasing demand of compute power has driven continuous scaling of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) which has been the fundamental force behind the microelectronics revolution, generating exponential growth in device density and performance as famously predicted by

Moore's Law [1] [2]. However, as channel lengths shrink into the nanometer regime, conventional bulk silicon CMOS technology starts to have fundamental physical limitations [1]. Short-channel effects (SCEs) such as threshold voltage roll-off, Drain-Induced Barrier Lowering (DIBL) and significant increases in subthreshold leakage currents severely lower device performance and increase static power consumption [3]-[5]. These challenges necessitate exploration of innovative device architectures to continue technological advancement at the same exponential rate.

A convincing alternative to address the obstacles of bulk silicon is Silicon-on-Insulator (SOI) technology [6]. By placing transistors on top of a thin silicon film that is dielectrically isolated from the substrate by a buried oxide (BOX) layer, SOI architectures offer inherent advantages, including the elimination of latch-up, reduced parasitic junction capacitances, and an improved subthreshold slope [5] [7]. Partially-Depleted (PDSOI) and Fully-Depleted (FDSOI) are the two types of SOI MOSFETs. PDSOI devices have a thicker silicon film (typically 100 nm to 200 nm), consisting of a neutral region in the device body that remains undepleted during operation [8]. This makes their threshold voltage less sensitive to film thickness variations, which also leads to an inherent Floating-Body Effect (FBE) [9] [10]. Impact ionization in PDSOI accumulates the majority charge carriers which raises body potential that results into a "Kink" in the output characteristics known as Kink Effect, it leads to transient instabilities that compromise performance in both the digital and analog domains [11].

Whereas, in FDSOI architecture, the entire body is depleted of mobile carriers during operation by utilizing an ultra-thin silicon film [12]. The neutral floating body is effectively eliminated in this architecture, thereby suppressing the kink effect and associated transient phenomena [7] [13]. The thin film and improved gate coupling give superior electrostatic integrity to FDSOI devices, which results in a near-ideal subthreshold swing, excellent control over SCEs, and reduced threshold voltage variability by using an undoped or lightly doped channel that mitigates random dopant fluctuations [12] [14]. These features establish FDSOI as a front runner for advanced low-power, low-voltage digital and analog applications.

As scaling progresses towards the sub 5 nm node, the role of gate stack becomes increasingly crucial for maintaining electrostatic control and minimizing power dissipation [15]. This intense scaling of gate oxide thickness (T_{GOX}) in conventional silicon dioxide (SiO_2) based devices leads to inconveniently high gate leakage currents due to direct quantum mechanical tunneling [4]. Which has warranted the use of high-permittivity (high-k) dielectric materials, that allow for a physically thinner film to suppress leakage while maintaining the same equivalent oxide thickness (EOT) for strong channel control [16]. Key device parameters, including threshold voltage, carrier mobility, and overall drive current, are directly influenced by the choice of GOX material [7] [17]. Although the fundamental advantages of FDSOI over PDSOI are well-documented, a detailed compara-

tive analysis at the 5 nm node that specifically investigates the performance trade-offs modulated by transitioning from ultra-thin SiO_2 to various high-k dielectrics is a critical area for investigation [16].

In this paper, a comprehensive simulation-based comparison of 5 nm gate length PDSOI and FDSOI n-MOSFETs is carried out, at first using an ultra-thin SiO_2 as gate oxide and then various high-k dielectric materials. Using the SILVACO ATLAS framework, we methodically analyze the impact of the gate oxide material on critical figures of merit, including I-V characteristics, I_{ON}/I_{OFF} ratio, threshold voltage and subthreshold slope. By directly comparing these two prominent SOI architectures, this study aims to unravel the complex interplay between device structure and gate stack engineering, generating helpful insights for the design and optimization of next-generation nanoscale transistors.

2. Methodology

2.1. Device Specification & Structure

Figure 1 illustrates a cross-sectional view of the investigated 5 nm FDSOI and PDSOI n-MSOFET. For both the FDSOI and PDSOI channel length was taken as identical, so that a fair comparison could be made. In Figure 1(a), Figure 1(b) the layout and placement of gate oxide, silicon layer, buried oxide, source and drain can be seen.

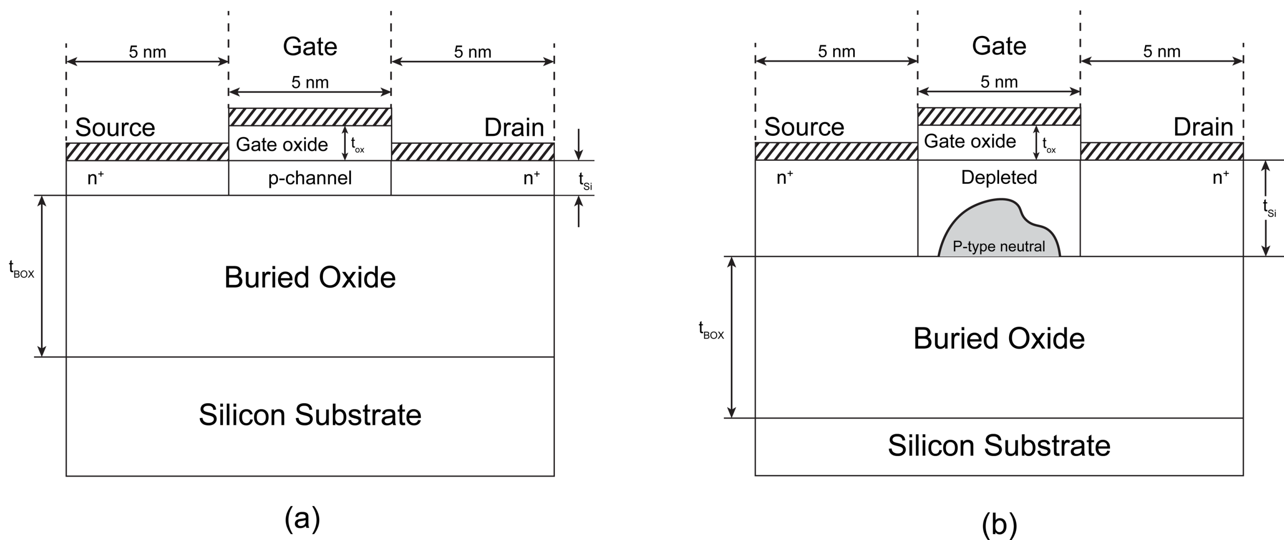

Figure 1. (a) 5 nm FDSOI Structure n-MOSFET (b) 5 nm PDSOI Structure n-MOSFET.

Major differences between the two devices occur in the silicon layer thickness (T_{Si}) and doping of the source, gate and drain regions. In FDSOI, an ultra-thin silicon layer was utilized to ensure better gate electrostatic control over the channel, which in turn helps to minimize leakage currents and Short-Channel Effects (SCEs) [18]. However, in PDSOI T_{Si} of significantly higher thickness was used as compared to FDSOI. Because it ensures that a floating body is created, which is the key characteristic of PDSOI, which supports higher drive current and dynamic

threshold operation [19].

From **Table 1**, all the devices take advantage of ultra-thin gate oxide thickness (T_{GOX}). In case of base FDSOI the silicon layer thickness (T_{Si}) used was 1.5 nm which is approximately 1/4th of the channel length, in optimized variant it was slightly reduced to 1.3 nm in optimized FDSOI. For PDSOI the T_{Si} was 7.5 nm for base variant and 8 nm for optimized variant. The T_{Si} of PDSOI variants was estimated by utilizing the Depletion Region Width Equation. Source and Drain doping concentrations for all 4 devices were taken as identical so that a comparative study could be executed as closely as possible. However, channel doping was dissimilar between PDSOI and FDSOI. A higher doping level (1×10^{20} cm^{-3}) was utilized in PDSOI to assist partial depletion, suppress punch-through and leakage. In contrast, a light doping level (1×10^{10} cm^{-3}) was used for FDSOI to ensure full depletion of the silicon film.

Table 1. Device specifications of base & optimized PDSOI and FDSOI.

Device Parameters	PDSOI (Base)	PDSOI (Optimized)	FDSOI (Base)	FDSOI (Optimized)
Gate Length, G_L (nm)	5	5	5	5
Silicon Layer Thickness, T_{Si} (nm)	7.5	8	1.5	1.3
Gate Oxide Thickness, T_{GOX} (nm)	0.5	0.4	0.5	0.5
Source & Drain Doping Conc.(n-type) (cm^{-3})	1×10^{21}	1×10^{21}	1×10^{21}	1×10^{21}
Channel Doping Conc. (p-type) (cm^{-3})	1×10^{20}	1×10^{20}	1×10^{10}	1×10^{10}
Gate Work function (eV)	4.5	4.5	5	4.9
Buried Oxide Thickness, T_{BOX} (nm)	33.5	33.5	33.5	33.5
Source and Drain Length (nm)	5	5	5	5

2.2. Device Simulation and Modelling

Silvaco TCAD ATLAS environment was used for device simulations and modelling of the 5 nm PDSOI & FDSOI devices. To capture the complex behavior of these nanoscale devices, an extensive set of physical models was employed in the simulation environment. The Auger Recombination model (AUGER), Shockley-Read-Hall (SRH) were employed for carrier recombination and generation mechanisms. Auger Recombination model was also used to evaluate high current densities. Bandgap narrowing due to heavy doping in source & drain regions was simulated by including Bandgap Narrowing Model (BGN). The concentration-dependent carrier mobility phenomenon was modelled using the Concentration-Dependent Mobility Model (CONMOB). In addition, the degradation of mobility in the inversion layer was simulated using the Lombardi (CVT) model. In ultra-scaled devices effect of lateral electric field on mobility, velocity saturation becomes significant, Field-Dependent Mobility Model (FLDMOB) was utilized to predict this phenomenon in the 5 nm long, 8 nm and 1.3

nm thick silicon channels in PDSOI and FDSOI respectively. Finally, Selberherr's impact ionization model (IMPACT SELB) was also utilized to account for short-channel effects which predict the breakdown characteristics of 5 nm devices. Different iterative numerical methods that are available in Silvaco TCAD were used to solve the devices in different biasing conditions. These arrays of models help to accurately capture the behavior of highly scaled SOI devices in this paper [20].

3. Results & Discussions

3.1. Parameters Investigated in FDSOI

In this section, 4 parameters were varied on the base variant of 5 nm FDSOI n-type MOSFET to estimate an optimized variant. In **Figure 2(a)**, T_{Si} varied from 1 nm to 3 nm, this showed that as the T_{Si} increases the corresponding curves shifts in the left. It means that as T_{Si} increases the threshold voltage (V_{th}) decreases, while the ON-current (I_{ON}) increases significantly. This happens because, with increasing T_{Si} the series resistance in the channel reduces whereas inversion charge density increases [21].

For **Figure 2(b)**, T_{GOX} varied from 0.1 nm to 1.7 nm. As T_{GOX} increases the corresponding I_{ON} decreases. Whereas the V_{th} slightly shifts toward the right which indicates that it increases but slightly. Thicker oxide decreases gate capacitance which results in weaker electric fields so less inversion charge that also means lower I_{ON}. Additionally, thicker T_{GOX} causes weaker gate control over the channel that means more voltage is required for inversion which increases the V_{th} [22]. In **Figure 2(b)**, a crossover of the graphs can be seen around 0.8 V. This occurred due to combined effects of V_{th} shift, sub-threshold swing (SS) variation, and dissimilar inversion charge dynamics which make thicker oxide devices lag the thinner oxide devices. Because thinner oxide devices reach inversion saturation before thicker oxide devices in same gate voltage conditions comparatively. **Figure 2(c)** shows I-V characteristics in case of different source & drain doping. With increasing doping, the I_{ON} current increases. Because channel's carrier conductivity increases with higher dopant [23]. Finally **Figure 2(d)** shows variation of Work function from 4.6 eV to 5.5 eV. With increasing value of Work function V_{th} increases because the gate needs higher voltage to overcome the increased energy barrier for forming inversion layer. On the contrary, I_{ON} decreases with increasing Work function for less gate overdrive due to higher V_{th}.

3.2. Parameters Investigated in PDSOI

This section varies the same parameters of the previous section on the base variant of 5 nm PDSOI n-type MOSFET to estimate an optimized variant. **Figure 3(a)** shows the effect of T_{Si} variation. Here, for T_{Si} above 7.5 nm the other 4 curves nearly overlap, this is because above a certain T_{Si} gate electric field is unable to influence the silicon body. That's why for 9 nm, 10.5 nm, 12 nm, 13.5 nm the T_{Si}

is overly thick to have any significant variation in drain current.

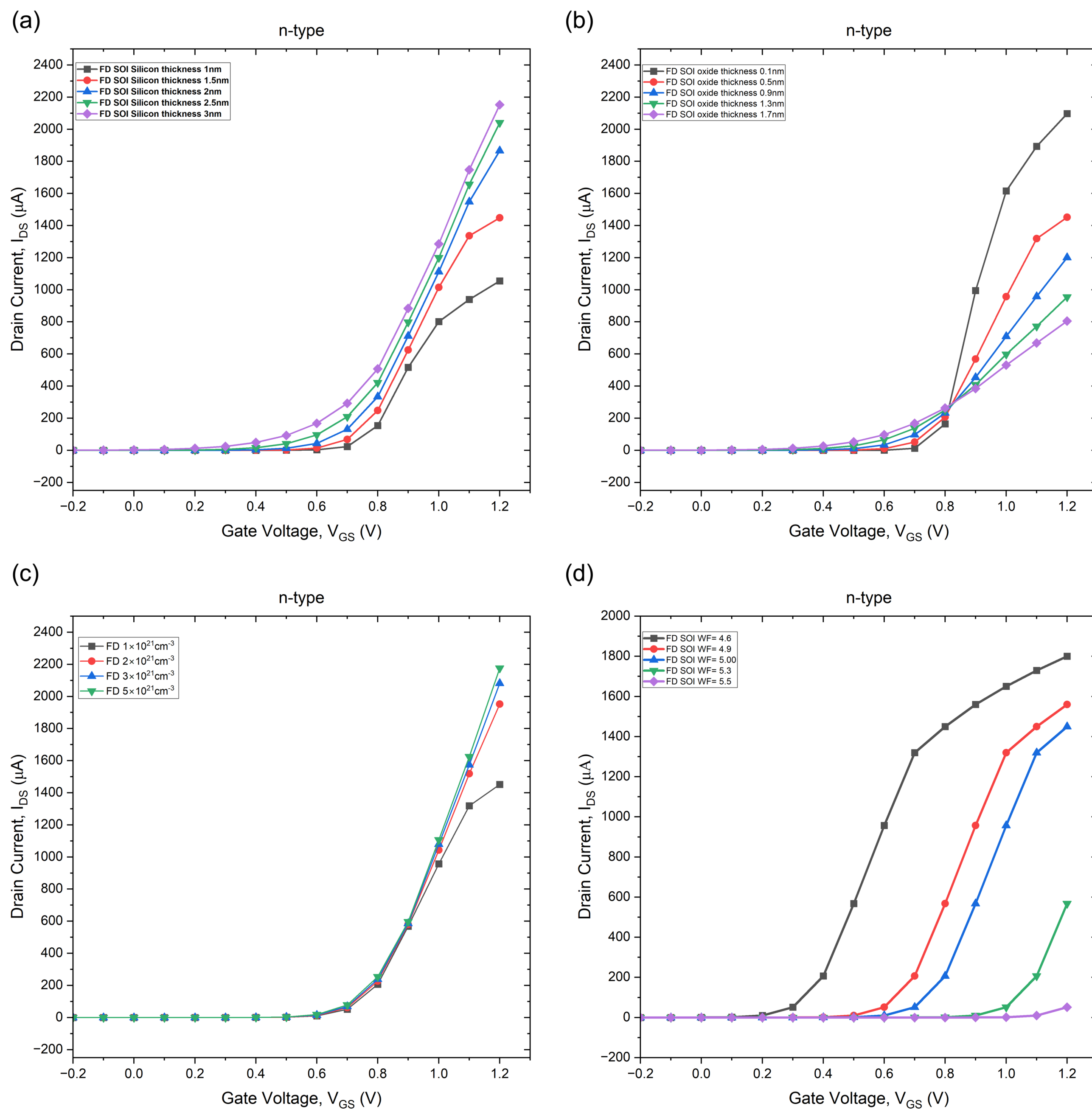

Figure 2. I_{DS} vs V_{GS} characteristics of 5 nm FDSOI (Base variant) for different parameter variations (a) Silicon thickness (b) Gate Oxide (c) Source & Drain doping (d) Work function.

In Figure 3(b) gate oxide thickness variation shows that for $T_{GOX} = 0.1$ nm where I_{ON} is higher than 5000 μA, which is nearly 2.3 times greater than FDSOI in Figure 2(b). This occurs due to the significant channel doping difference between the two types of devices as shown in Table 1. Other trends in the graph are like Figure 2(b). Figure 3(c), Figure 3(d) vary source & drain doping, Work function. And the trends of the curves are similar to those in Figure 2(c), Figure 2(d).

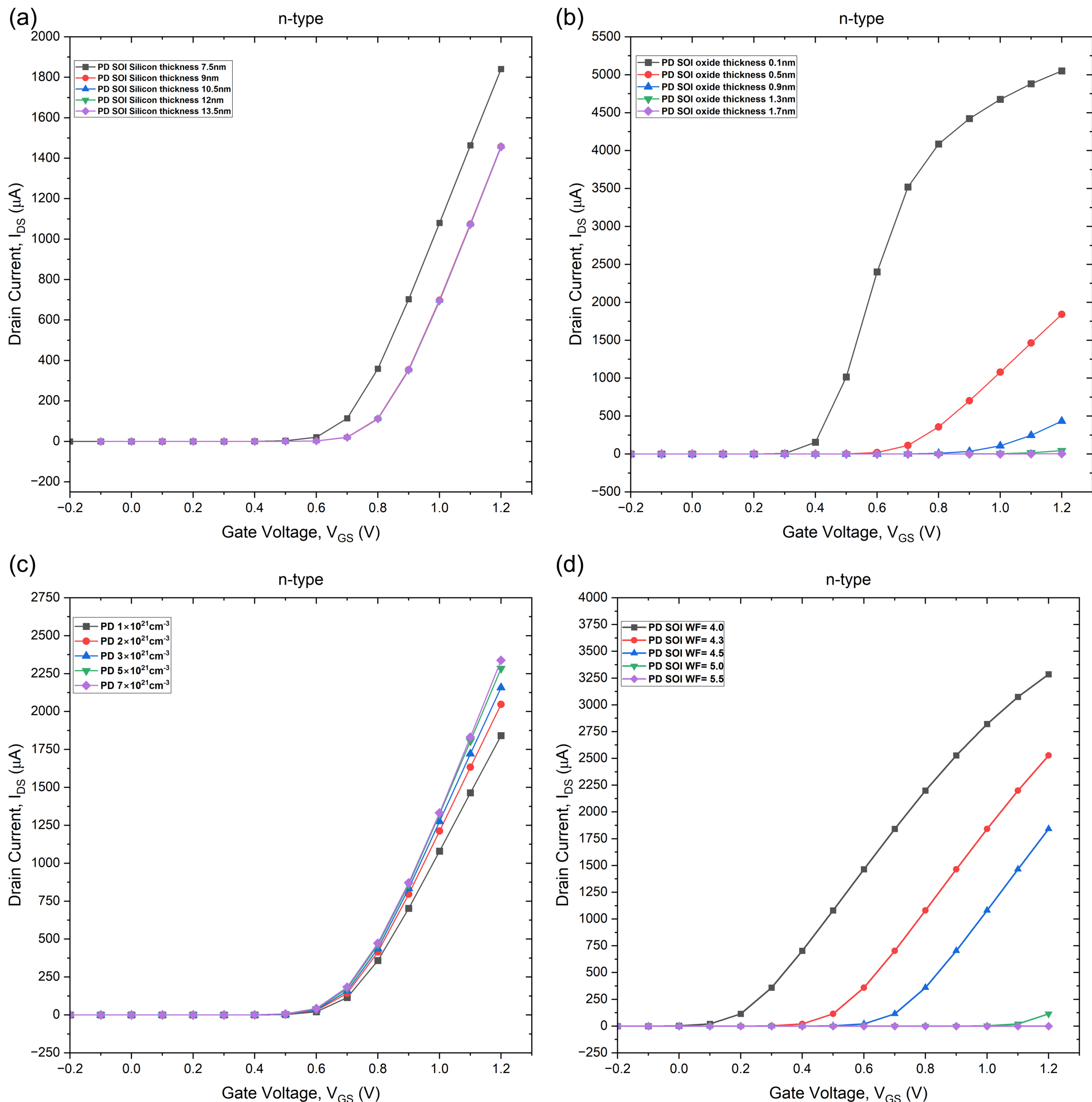

Figure 3. I_{DS} vs V_{GS} characteristics of 5 nm PDSOI (Base variant) for different parameter variations (a) Silicon thickness (b) Gate Oxide (c) Source & Drain doping (d) Work function.

3.3. Optimized FDSOI & PDSOI n-MOSFETs

Figure 4 & Figure 5 focus on the comparison of I_{DS}/V_{GS} characteristics & SS of optimized variants of the devices. From Figure 4 and Table 2 in case of PDSOI variants, there was a 17.04% and 15.78% reduction in V_{th} and sub-threshold slope, respectively.

For FDSOI variants from Figure 5 and Table 2, there was a reduction of 6.6% and 11.04% reduction in V_{th} and SS respectively. Lower V_{th} facilitates lower power consumption and better performance. Comparison between investigated opti-

mized variants of PDSOI and FDSOI shows that the PDSOI device had lower V_{th} and SS slope. This is because the changes in design parameters have greater influence on V_{th} and SS in PDSOI. Whereas in FDSOI it is more stable when changing the design criteria.

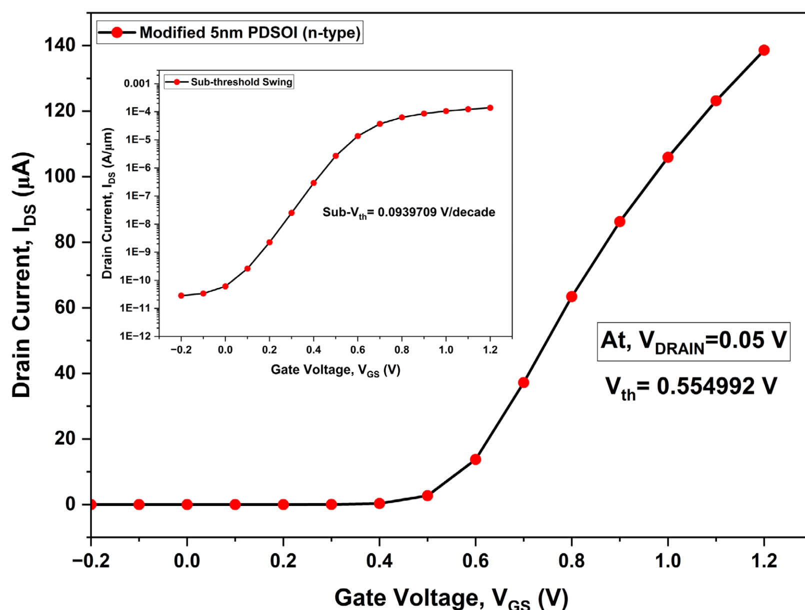

Figure 4. I_{DS} vs V_{GS} characteristics of 5 nm PDSOI (Optimized variant).

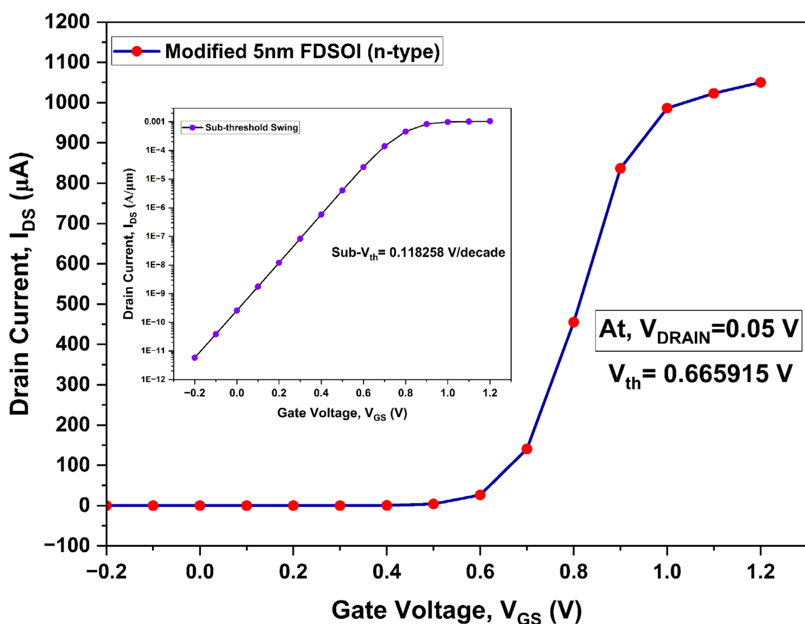

Figure 5. I_{DS} vs V_{GS} characteristics of 5 nm FDSOI (Optimized variant).

Leakage current for both PDSOI and FDSOI were lower than expected in spite of short channel effects. The I_{DS} was 1.049542 mA at 1.2 V for FDSOI (optimized) which is higher than the PDSOI (optimized), this results in higher Power Consumption, stronger drive strength & better signal integrity. In **Figure 5** slope of

the curve significantly decreases after 1 V compared to in the range of 0.6 V to 1 V. This FDSOI (optimized) with further increase in $V_{GS,}$ the I_{DS} output curve tapers. But the PDSOI (optimized) the I_{DS} increases nearly in a proportional manner with increasing V_{GS}, demonstrating linear dependency in the strong inversion region. This difference arises due to partially-depleted and the fully-depleted SOI region.

Table 2 shows different performance parameters of base and optimized variants for both PDSOI and FDSOI. I_{ON}/I_{OFF} ratio for all variants is in the range of 10^6 indicating highly efficient switching performance. This demonstrates excellent gate control and sub-threshold characteristics, which are crucial for high-performance devices.

Table 2. Performance parameters of base and optimized variants of PDSOI and FDSOI.

Device Parameters	PDSOI (Base)	PDSOI (Optimized)	FDSOI (Base)	FDSOI (Optimized)
Threshold Voltage, Vth(V)	0.669009	0.554992	0.712988	0.665915
Sub-threshold Swing, SS (mV/decade)	111.708	93.9709	132.934	118.258
Drain Current, I_{ON} (A)	1.840772×10^{-3}	1.386755×10^{-4}	1.452111×10^{-3}	1.049542×10^{-3}
Leakage Current, I_{OFF}(A)	6.441692×10^{-10}	6.08135×10^{-11}	3.427677×10^{-10}	1.995262×10^{-10}
I_{ON}/I_{OFF} (A)	2.85759×10^{6}	2.280342×10^{6}	4.236428×10^{6}	5.260173×10^{6}

Figure 6 shows comparison of Electric Field profile for optimized PDSOI and FDSOI devices. For both cases there was sharp increase in magnitude of electric field near the source edge (0.005 μm) and a similar decrease near the drain edge (0.01 μm).

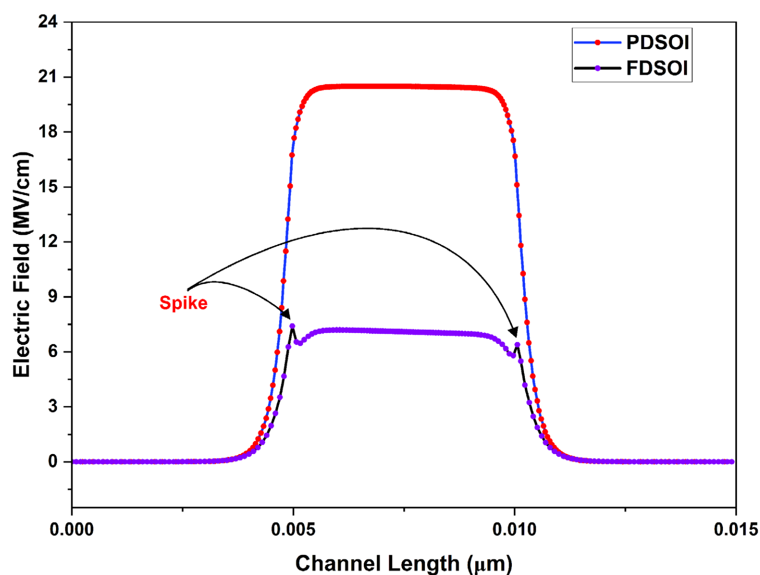

Figure 6. Electric field vs Channel Length profile of Optimized variants of PDSOI and FDSOI.

The PDSOI curve peaks at around 20 MV/cm and FDSOI around 7 MV/cm. Thicker silicon body of PDSOI lets larger lateral fields to develop enables boosting of ON-current drive. On the contrary, thin silicon body of FDSOI causes stronger gate coupling which limits field strength but improves electrostatic integrity. Spikes in the FDSOI curve are due to abrupt change in doping profiles of source-channel and channel-drain interface.

3.4. Kink Analysis

Figure 7 shows I_D vs V_D curves for increasing gate voltages (V_g) which is used to analyze Kink Effect in MOSFETs. The PDSOI MOSFET (optimized) in **Figure 7(a)** shows kink after V_D = 4.77 V whereas for FDSOI in **Figure 7(b)** no kink was seen for the range of applied voltages.

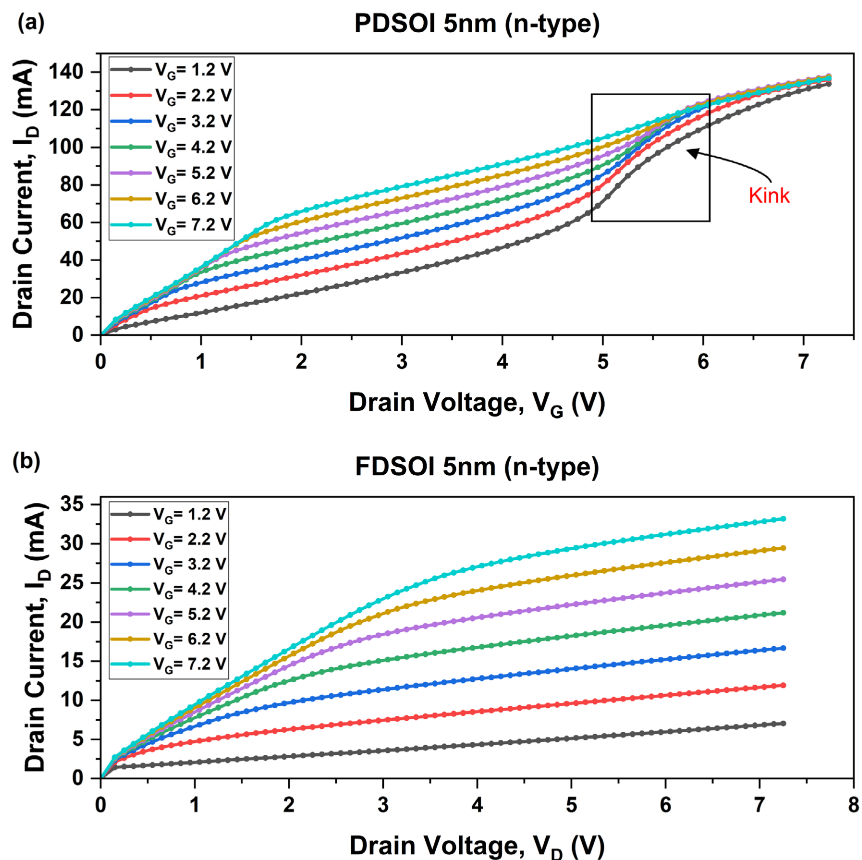

Figure 7. I-V curve for Drain Voltage of 7.2 V for optimized variant of (a) PDSOI (b) FDSOI.

In **Figure 7(a)**, we can see kink appears in the PDSOI I_D-V_D graph, it is a direct manifestation of the floating-body effect. With increasing the drain voltage (V_D), high lateral electric field near the drain results in impact ionization for creating an electron-hole pair. As the electrons are attracted towards the drain, the created holes are pushed into the neutral floating body region [9] [24]. The accumulation of these holes increases the potential level in the body, and thus reduces (V_{th}). This

decrease in V_{th} facilitates the abrupt surge of the I_D, which results in a "kink" feature at about 4.77 V. But in FDSOI the fully-depleted thin body eliminates charge buildup that prevents any kink effect [25] [26].

3.5. GOX Variation Analysis

Various Gate Oxide materials were explored in search of better device characteristics as shown in **Figure 8**. Default material parameters of Silvaco TCAD (version 2016) were utilized for simulations of different gate oxide materials [20].While these parameters are widely used and provide reliable comparative insights, they may not fully capture process-dependent variations, interface trap densities, and material imperfections which may result in discrepancies with fabricated high-k/Si gate stacks. For PDSOI in **Figure 8(a)** there is much variation in V_{th} and I_{DS} but for FDSOI in **Figure 8(b)** the curves are much closer showing less variation. This is due to partial depletion effects and weaker electrostatic gate control in PDSOI and superior electrostatic gate control in FDSOI. Using high-k materials such as Ta_2O_5, HfO_2, ZrO_2 shows lower V_{th} and sub-threshold swing (SS) compared to other materials for PDSOI (from **Table 3**).

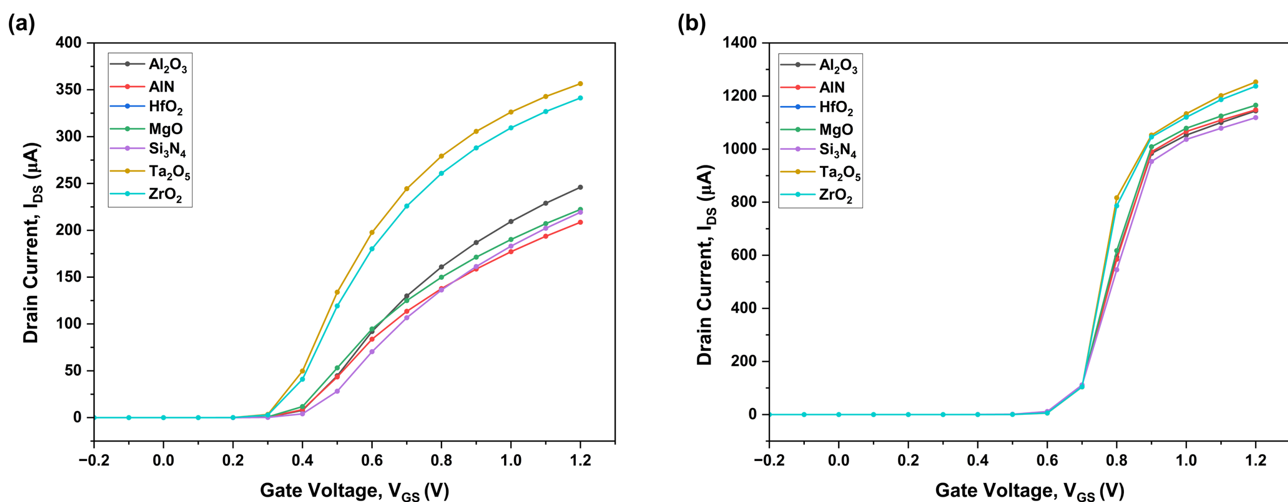

Figure 8. I_{DS} vs V_{GS} graph for different Gate Oxide materials of (a) optimized PDSOI (b) optimized FDSOI.

Table 3. Performance parameters of optimized PDSOI for various gate oxide materials.

Device Parameters	Ta_2O_5	HfO_2 & ZrO_2	AlN	Al_2O_3	MgO	Si_3N_4
Threshold Voltage, Vth(V)	0.337716	0.344554	0.388994	0.402176	0.368956	0.430226
Sub-threshold Swing, SS (mV/decade)	69.0701	69.8288	75.8425	76.2472	74.3786	78.9954
Drain Current, I_{ON} (A)	3.564511×10^{-4}	3.411929×10^{-4}	2.08449×10^{-4}	2.460367×10^{-4}	2.223309×10^{-4}	2.192804×10^{-4}
Leakage Current, I_{OFF} (A)	2.167704×10^{-10}	1.981527×10^{-10}	1.1324×10^{-10}	1.114294×10^{-10}	$1.2445146 \times 10^{-10}$	9.484184×10^{-11}
I_{ON}/I_{OFF} (A)	1.644371×10^6	1.721868×10^6	1.840772×10^6	2.208×10^6	1.786487×10^6	2.312064×10^6

In PDSOI V_{th} was 39.15%, 37.92% and 22.48% better for Ta_2O_5, HfO_2/ZrO_2 and Si_3N_4 respectively than SiO_2 (For optimized variant in Table 2 and Table 3). For FDSOI V_{th} was 0.826%, 0.937% and 2.496% better for Ta_2O_5, HfO_2/ZrO_2 and Si_3N_4 respectively than SiO_2 (For optimized variant in Table 2 and Table 4). FDSOI exhibits much better I_{ON}/I_{OFF} ratio compared to PDSOI (around 10^9 and 10^6 range in FDSOI and PDSOI respectively) for same set of gate oxide materials (from Table 3 and Table 4).

Table 4. Performance parameters of optimized FDSOI for various gate oxide materials.

Device Parameters	Ta_2O_5	HfO_2 & ZrO_2	AlN	Al_2O_3	MgO	Si_3N_4
Threshold Voltage, Vth(V)	0.660409	0.65967	0.651549	0.652359	0.653326	0.649291
Sub-threshold Swing, SS (mV/decade)	78.0335	79.5596	92.4006	90.8435	89.5885	95.7378
Drain Current, I_{ON} (A)	1.2531411×10^{-3}	1.2359474×10^{-3}	1.1481536×10^{-3}	1.1428783×10^{-3}	1.164126×10^{-3}	1.119437×10^{-3}
Leakage Current, I_{OFF} (A)	$1.6904409 \times 10^{-13}$	2.333458×10^{-13}	4.017908×10^{-12}	2.904022×10^{-12}	2.333458×10^{-12}	7.095777×10^{-12}
I_{ON}/I_{OFF} (A)	7.413102×10^{9}	5.296634×10^{9}	2.85759×10^{8}	3.935501×10^{8}	4.988844×10^{8}	1.5776101×10^{8}

4. Conclusions

This work demonstrates a comparative study between PDSOI and FDSOI n-MOSFETs in 5 nm node with parameter analyses to improve performance characteristics by changing gate oxide materials. In the designed n-MOSFETs when gate oxide is SiO_2, PDSOI has lower V_{th} (0.554 V), SS (93.97 mV/decade), I_{OFF} (6.08135×10^{-11} A) and FDSOI has higher I_{ON} (1.049542×10^{-3} A), I_{ON}/I_{OFF} ratio (5.260173×10^6). Analysis of electric fields along the channel revealed stronger fields in PDSOI than FDSOI. I_D vs V_D graph for different V_g shows that PDSOI experience kink at the vicinity of 4.77 V drain voltage but in FDSOI no such kink was observed.

Substituting SiO_2 with high-k materials such as Ta_2O_5 and HfO_2 significantly improved SS for both PDSOI (69 mV/decade) and FDSOI (78 mV/decade). With Ta_2O_5 as gate material the PDSOI device achieves high drive current of 3.56×10^{-4} A and linear dependency in the strong inversion region as shown in Figure 4 which makes it suitable for nueromorphic hardwares and in-memory computation. The FDSOI device shows huge I_{ON}/I_{OFF} ratio of 7.4×10^9 and ultra-low leakage current of 1.69×10^{-13} A (when using Ta_2O_5), exhibiting its potential applications for ultra-dense AI accelerators and wearable electronics. These 5 nm PDSOI and FDSOI n-MOSFETs with their low V_{th}, sharp subs-threshold swing, high ON-current and exceptionally low leakage current makes it suitable for application where low power consumption and high switching efficiency is of great importance. Application areas may include in-memory computation, neuromorphic

hardware, ultra-dense AI accelerators, wearable electronics, implantable bio-medical devices, IoT devices and others.

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Author Contributions

Md. Muntasir Alam: Conceptualization, Initial Framework, Methodological Implementation, Simulation Execution. **Md. Asif Rahman:** Conceptualization, Initial Framework, Methodological Implementation, Simulation Execution. **Anika Tahasin Parisa:** Visualization, Writing - Original Draft Preparation, Revisions. **Dr. Towhid Adnan Chowdhury:** Writing - review & editing, Supervision, Formal Analysis. All authors read and approved the final manuscript.

Data Availability

The data generated and analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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