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Design and Implementation of a Closed-Loop Single-Phase Transistor-Clamped H-Bridge Multilevel Inverter Using FPGA

Wahidah Abd Halim[1*], Nurul Ain Mohd Said[1], Maaspaliza Azri[1], Azrita Alias[1], Siti Rohani Sheikh Raihan[2]

[1]Faculty of Electrical Technology and Engineering, Universiti Teknikal Malaysia Melaka, Melaka, Malaysia
[2]Higher Institution Centre of Excellence (HICoE), UM Power Energy Dedicated Advanced Centre (UMPEDAC), Universiti Malaya, Kuala Lumpur, Malaysia

Email: *wahidahhalim@utem.edu.my

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Abstract

This paper presents the performance evaluation of a single-phase five-level transistor-clamped H-bridge (TCHB) inverter, which is a modified circuit based on H-bridge inverter topology involving closed-loop control. The modulation technique used here is multicarrier sinusoidal pulse-width modulation. The single-phase five-level TCHB inverter simulation model is constructed using MATLAB/Simulink software. In addition, a single-phase conventional H-bridge inverter simulation model using bipolar and unipolar switching schemes, which generates both two levels and three levels of output voltage, is also constructed in MATLAB/Simulink. The total harmonic distortion (THD) results for the two-level, three-level, and five-level inverters are analysed and compared; it is found that the THD for the higher-level inverter is lower. The obtained simulation results are then analysed and discussed. The hardware prototype of the single-phase five-level TCHB inverter is constructed, and analysis is carried out using field programmable gate array (FPGA). The results show that the presented five-level TCHB inverter can produced a sinusoidal output voltage with low harmonic distortion as the amplitude modulation ratio increases.

Keywords

Multilevel Inverter, Multicarrier Sinusoidal Pulse-Width Modulation, Total Harmonic Distortion, Field Programmable Gate Array

1. Introduction

The inverter is a power electronic device which converts DC power to AC power. Inverters are widely used in many types of applications, including renewable energies—especially photovoltaic (PV) and fuel cells [1] [2]—adjustable-speed drives [3], uninterruptible power supplies (UPS) [4], and more. The earliest inverter topology invention is a two-level inverter [5] [6]; since the output voltage is not close to a sinusoidal wave shape, this topology is only suitable for application in industrial applications and power systems which require low power quality. This topology has evolved to a multilevel inverter topology, due to its bad performance when operating in high power and medium-/high-voltage applications at high switching frequency. The idea of the "multilevel inverter" was introduced in 1975, beginning with the three-level inverter [7] [8].

Multilevel inverters have attracted the interest of researchers and academia, given that they are crucial in high-power and high-voltage applications as a result of their ability to deliver higher output voltage quality compared to traditional two-level inverter topologies. Multilevel inverters are reported to produce superior output voltage quality, as the generated output voltage takes a staircase form which closely approximates a sinusoidal waveform shape with an increasing number of levels [7]-[16]. The smoothness of the output voltage waveform can be enhanced by increasing the number of levels in the multilevel inverter, which consequently reduces the total harmonic distortion (THD) in the output waveform.

Many types of multilevel inverter topologies have been introduced [9] [10], with the three primary topologies being diode-clamped or neutral point clamped, flying capacitor, and cascaded H-bridge. Recently, attention has been directed to minimising the number of components in multilevel inverters to reduce voltage stress, lower harmonic distortion, lower switching frequency and switching losses, and improve efficiency in both single-source and multiple-source configurations, as described in [10]. However, as the number of output voltage levels increases, a greater number of switches, DC sources, gate driver circuits, heat sinks, and protective components are required; this leads to higher costs and greater control system complexity.

Researchers have introduced numerous forms of modulation approaches for multilevel inverters. These modulation techniques are classified into two categories: low switching frequency modulation techniques and high switching frequency modulation techniques. Examples of low switching frequency modulation techniques include selective harmonic elimination (SHE) [11], nearest vector control (NVC), and nearest level control (NLC) [12], whereas high switching frequency modulation techniques include multireference or multicarrier pulse-width modulation (PWM) [13]-[15] and space vector modulation (SVM) [16]. Hybrid modulation refers to the integration of the two types of modulation techniques.

Field programmable gate arrays (FPGAs) have been widely implemented in power electronics systems due to their flexibility, high processing speed, and ca-

pability to execute complex control algorithms in real time [17]-[25]. Although FPGA-based controllers have been extensively applied in various power electronics systems—such as DC-DC converters [18] [19], inverters [20]-[23], rectifiers [24], and cycloconverters [25]—limited research focuses on closed-loop single-phase transistor-clamped H-bridge (TCHB) multilevel inverter systems using FPGA. Existing studies primarily address conventional multilevel inverter topologies or emphasise simulation-based analysis, with minimal hardware validation for TCHB configurations with FPGA integration specifically. This gap highlights the need for experimental performance evaluation of single-phase TCHB multilevel inverters controlled by FPGA, to enhance their applicability in real-world power conversion systems.

While FPGAs have been widely used in other power electronic applications, their role in this work extends to real-time implementation of a discrete proportional-integral (PI) controller, enabling fast dynamic response, precise switching control, and reduced harmonic distortion. Therefore, the novelty of this work lies in the integration of FPGA-based closed-loop control for the single-phase five-level TCHB inverter topology. To the best of our knowledge, this is the first reported study that experimentally validates a closed-loop TCHB multilevel inverter using FPGA, addressing a gap in prior research that has largely been limited to simulation or conventional inverter topologies.

In this context, the TCHB multilevel inverter emerges as a more effective alternative to conventional multilevel topologies. The diode-clamped inverter requires a large number of clamping diodes, leading to higher switching losses and increased design complexity. The flying capacitor topology demands numerous capacitors, which not only raises system cost but also introduces reliability concerns. Similarly, the cascaded H-bridge inverter depends on multiple isolated DC sources, limiting its suitability for compact applications. In contrast, the TCHB multilevel inverter achieves the same level output with fewer switches and DC power supplies, thereby simplifying the hardware design while maintaining efficient and reliable performance.

This paper presents the detailed design of a multicarrier sinusoidal pulse-width modulation (SPWM) technique in order to produce five distinct voltage levels in the TCHB multilevel inverter. The closed-loop system of the TCHB multilevel inverter is first modelled and simulated in MATLAB/Simulink; this is followed by the development and testing of a hardware prototype controlled using FPGA. The performance of the TCHB multilevel inverter, obtained from both the simulation and the experimental implementation, is then evaluated and compared with that of a conventional H-bridge inverter.

2. The Proposed Inverter Topology and Its Operation

Figure 1 illustrates the five-level TCHB inverter configuration, which comprises a conventional H-bridge inverter with an auxiliary switch and four diodes functioning as bidirectional switches connected to the centre of the DC capacitors.

With appropriate switching management, the auxiliary switch will be capable of generating half the level of the DC supply voltage, or ±1/2 V_{dc}.

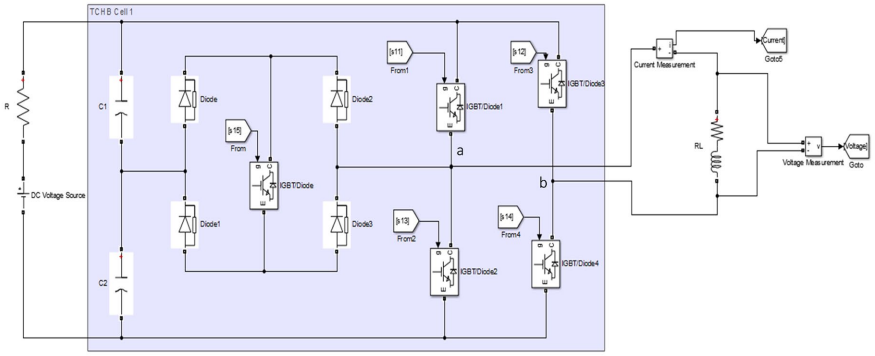
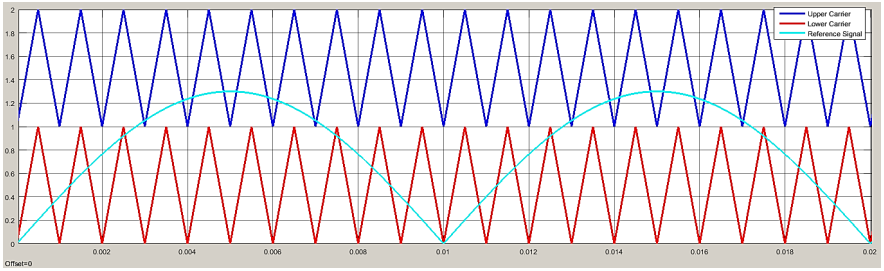
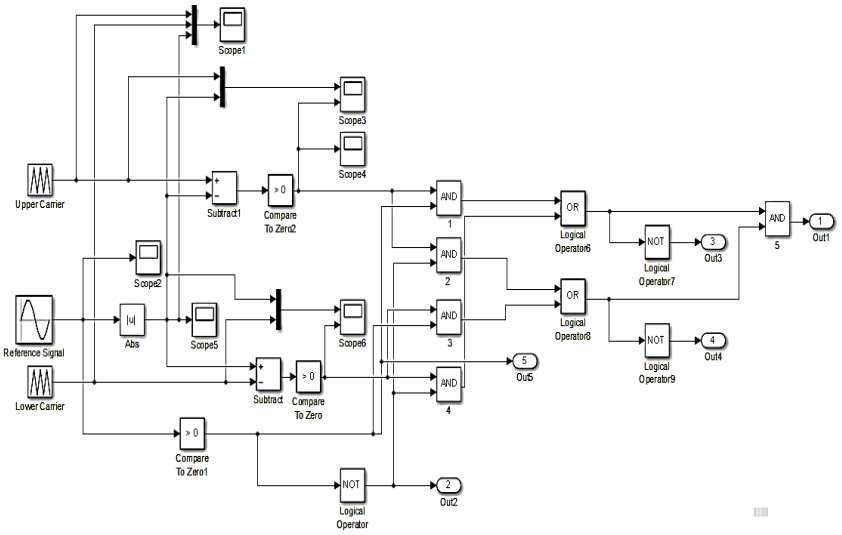


Figure 1. The five-level TCHB inverter topology.



(a)



(b)

Figure 2. Modulation technique for the five-level TCHB inverter: (a) Multicarrier SPWM; (b) PWM signal generation.

The multicarrier SPWM technique used here compares the sinusoidal reference waveform with the triangular waveform of the carrier signals to generate the PWM switching signals. Two triangular carrier signals and one reference sinusoidal signal are used for multicarrier SPWM signal generation for the five-level TCHB in-

verter, as illustrated in Figure 2(a). The reference sinusoidal signal has a frequency of 50 Hz. The negative waveform of the reference sinusoidal signal is lifted using the modulus block in MATLAB/Simulink, as illustrated in Figure 2(b). In a comparison of the reference sinusoidal signal with the upper and lower sides of the triangular carrier signals, the PWM switching signals are generated through the application of combinational logics.

The amplitude modulation ratio M_a of the proposed five-level TCHB inverter can be expressed as:

$$M_a = \frac{A_M}{2A_C} \tag{1}$$

where A_M is the reference signal's peak value, while A_C is the peak-to-peak value of the carrier signals used. The behaviour of the evaluated five-level TCHB inverter is obtained when the modulation index is more than 0.5 but less than or equal to 1 ($0.5 < M_a \leq 1$). If the modulation index is equal to or less than 0.5 ($0.5 \leq M_a$), the behaviour of the proposed inverter mimics that of a three-level inverter; this was due to only the lower carrier wave being compared with the reference signal, and thus the output voltage produced is only half the DC bus voltage. When the amplitude of the reference signal exceeds the amplitude of the upper carrier wave and the modulation index is greater than 1 ($M_a > 1$), over-modulation occurs.

Table 1. Switching states and output voltage of the five-level TCHB Inverter.

S_1	S_2	S_3	S_4	S_5	v_{inv}
1	0	0	1	0	$+V_{dc}$
0	0	0	1	1	$+\frac{1}{2}V_{dc}$
0	0	1	1	0	0
1	1	0	0	0	0
0	1	0	0	1	$-\frac{1}{2}V_{dc}$
0	1	1	0	0	$-V_{dc}$

1: ON; 0: OFF.

Table 1 shows the output levels of TCHB inverter based on the operational condition of the switches, which were either 1 (on) or 0 (off). This topology can generate five different levels of output voltage waveforms: $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$. Only two switches are operated at one time. Through the combinations of the on and off states of the switches (S_1 - S_5) depicted in Table 1, the inverter output voltage v_{inv} can be expressed as:

$$v_{inv} = V_{dc}\left(S_4 - S_2\right)\left\{\frac{1}{2}S_5 + \left|S_1 - S_2\right| \cdot \left|S_3 - S_4\right|\right\} \tag{2}$$

The proposed five-level TCHB inverter is a buck converter whose average out-

put voltage v_o is characteristically always lower than the input DC voltage V_{dc}. Equation (3) gives the peak value of the proposed inverter's output voltage:

$$v_o = M_a V_{dc} \tag{3}$$

3. Closed-Loop Control Implementation Using FPGA

The FPGA used for hardware development is the Altera DE2 Board. The advantages of DE2 FPGA include affordability, many flexible onboard features, freedom in designing both hardware and CAD tools, and the ability to implement a wide range of digital circuit designs. A Cyclone II 2C35 FPGA device is included together with the aid of various hardware resources and components incorporated on-board, including 33,216 logic elements (LE), 483,840 RAM bits, 35 embedded multipliers, and 475 user I/O pins.

The main goal of the control strategy for the proposed TCHB multilevel inverter is the production of sinusoidal output voltage with low harmonic distortion under proper control techniques. A proportional–integral (PI) control algorithm is implemented as the feedback controller for the proposed inverter. A basic closed-loop feedback system with a PI controller for the inverter may include a sensor, an analog-to-digital converter (ADC), and a digital PWM as shown in Figure 3. The PI controller feeds on the error between the reference voltage and the measured output voltage. If $y(t)$ is the measured variable and $r(t)$ is the reference variable, the error $e(t)$ is:

$$e(t) = r(t) - y(t) \tag{4}$$

In continuous time, the input $e(t)$ and the output $u(t)$ of the PI algorithm relate as follows:

$$u(t) = K_p e(t) + K_i \int_0^t e(t)\,\mathrm{d}\tau \tag{5}$$

where K_p and K_i are the proportional gain and the integral gain, respectively.

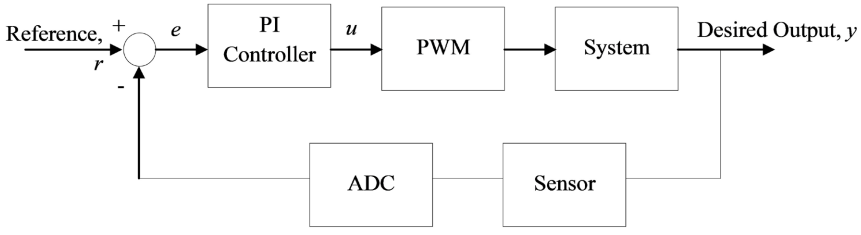


Figure 3. Closed-loop system with PI controller.

The PI control algorithm is designed in a discrete form to enable implementation on FPGA. By applying the Tustin approximation, the integral term is discretized, and the discrete PI controller can be expressed as:

$$U(z) - U(z)z^{-1} = K_1 E(z) + K_2 E(z)z^{-1} \tag{6}$$

where $K_1 = \left(K_p + \frac{K_i T_s}{2}\right)$ and $K_2 = \left(\frac{K_i T_s}{2} - K_p\right)$

The desired output response is achieved by tuning the K_p and K_i gains of the PI controller. After the tuning process is done, with $K_p = 10$, $K_i = 1$ using $T_s = 1$ μs sampling time, the discrete PI controller is implemented as:

$$u(n) = u(n-1) + 10.0000005e(n) - 9.9999995e(n-1) \quad (7)$$

To ensure stable operation, the PI controller must be protected against integral windup which is undesired condition by preventing the integral value from exceeding the required limit.

An appropriate ADC must be chosen to convert the analogue voltage signal into digital, as there is no integrated ADC on the DE2 FPGA board, and the selected ADC chip should be inexpensive. The feedback signal from the inverter or the measured voltage is sensed by a voltage sensor (LV25-P) and then fed at an 8-kHz sampling rate to an ADC0808 (8-bit). The measured (digital) voltage is then compared with the sinusoidal lookup table (LUT) (the sine-wave reference), with the resultant signal subsequently fed to the digital PI controller. The implementation of digital PI controller using FPGA is illustrated in Figure 4.

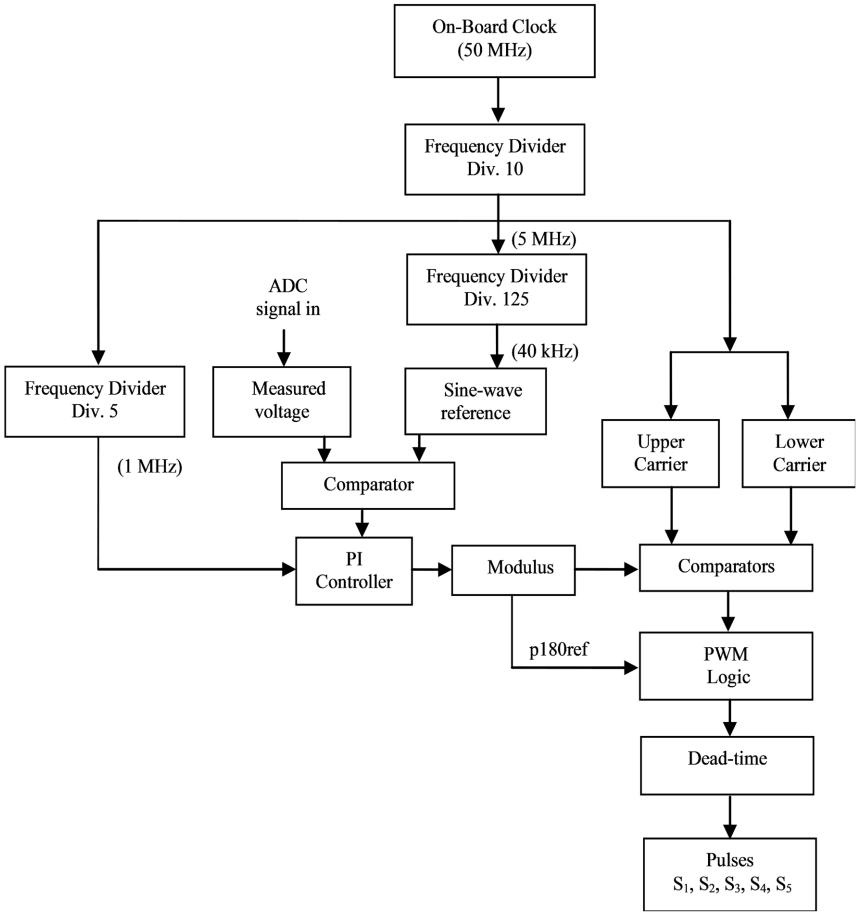
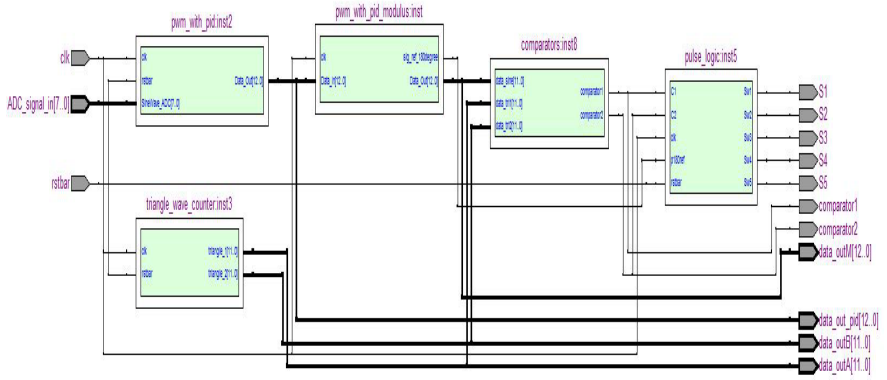


Figure 4. Implementation of closed-loop system with PI controller using FPGA.

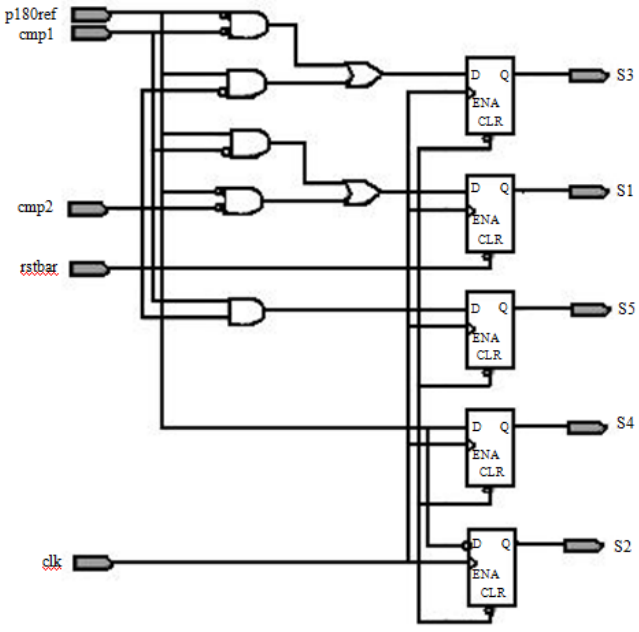
To prevent a short circuit across the input voltage source, the dead-time t_{dead} is included in the gating signals of the switches. (Dead-time is usually called delay

time or blanking time.) For practicality, these signals are given to the gate driver circuit to trigger the switching devices (insulated gate bipolar transistors, or IGBTs). The magnitude of t_{dead} is set to 1 μs and applied between the PWM signals.

The FPGA-based PWM generator is designed using Verilog HDL and through schematic design entries. The design, synthesis, and simulation are conducted on Quartus Prime software. Five PWM output signals with dead-time are assigned and sent to the gate drive circuit to trigger the proposed inverter circuit. In addition, the Quartus Prime software includes a tool for the designer to view the designed circuit in schematic diagram through register transfer level (RTL) Viewer; the RTL graphics are presented for the design of the PWM generator with a PI control algorithm—shown in Figure 5(a)—and the PWM logic module—illustrated in Figure 5(b).



(a)



(b)

Figure 5. FPGA implementation: (a) Top-level design of PWM generation with the PI controller; (b) RTL design of the PWM logic block.

4. Results and Discussion

4.1. Simulation Results

In order to compare the THD of two-level, three-level, and five-level inverters, a conventional H-bridge inverter with bipolar and unipolar switching schemes is constructed in MATLAB/Simulink. In addition, the conventional H-bridge inverter is improved by adding a bidirectional switch, comprising one switch (S_5) and four diodes located at the midpoint of the DC-link capacitors for a TCHB inverter topology. The parameters used for the two-level and three-level conventional H-bridge inverter, and for the five-level TCHB inverter, are shown in Table 2.

Table 2. The parameters of the five-level TCHB inverter configuration.

Parameters	Values
DC voltage source, V_{dc}	400 V
Switching frequency, f_{sw}	20 kHz
Amplitude modulation ratio M_a	0.4 - 1.0
Capacitors, C_1, C_2	2200 μF
Inductor filter, L_f	12 mH
Resistor load, R	100 Ω

Figure 6 presents the PWM gating signal results generated from Quartus Prime software, with switching patterns for the five-level TCHB inverter observed at an amplitude modulation ratio M_a of 0.85. The result shows that switches S_1, S_3, and S_5 function at carrier-signal frequency, while switches S_2 and S_4 function at reference frequency as designed (see Figure 2(b)). Figures 7(a)-(c) illustrate the inverter output waveforms, with an amplitude modulation ratio M_a of 0.85 for the two-level inverter, three-level inverter, and five-level TCHB inverter, respectively.

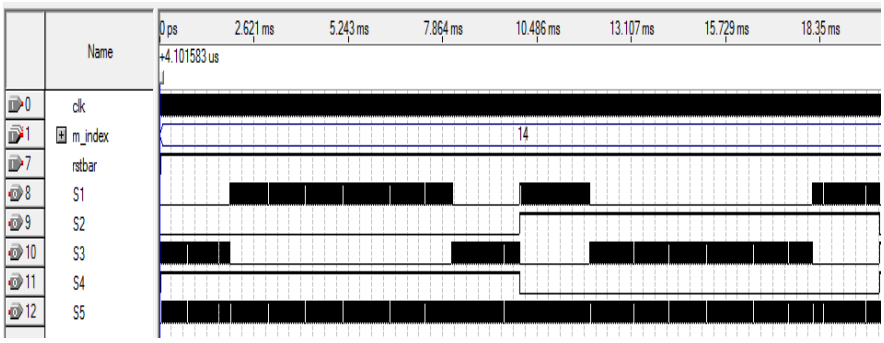
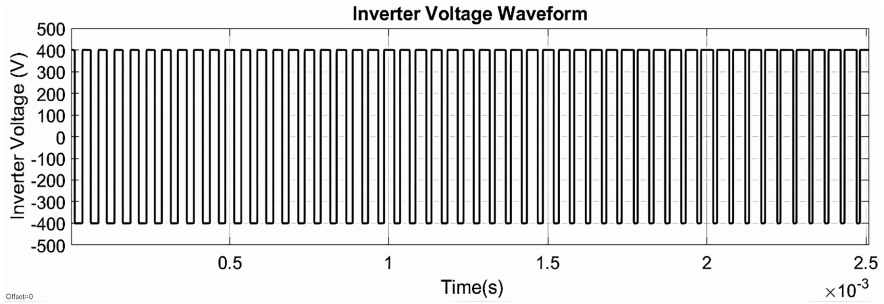


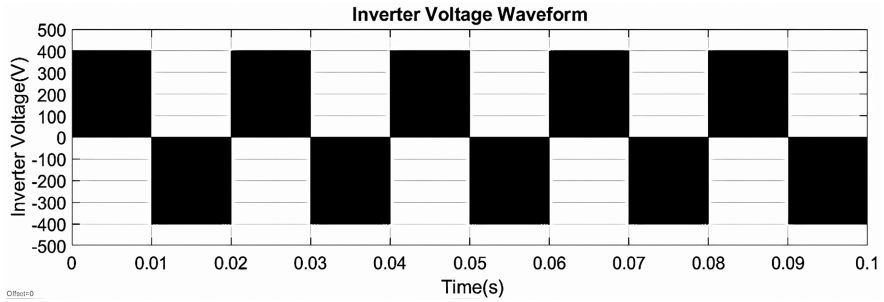
Figure 6. Switching pattern for the five-level TCHB inverter.

A bipolar single-phase conventional H-bridge inverter generates two output voltage levels: 400 V and −400 V; it is often referred to as a two-level inverter. At the same time, a unipolar single-phase conventional H-bridge inverter generates

three output voltage levels: 400 V, 0 V, and −400 V; due to these three levels of output, it is referred to as a three-level inverter. The simulation results reveal that the TCHB inverter voltage waveform exhibits five distinct levels: 400 V, 200 V, 0 V, −200 V, and −400 V.



(a)



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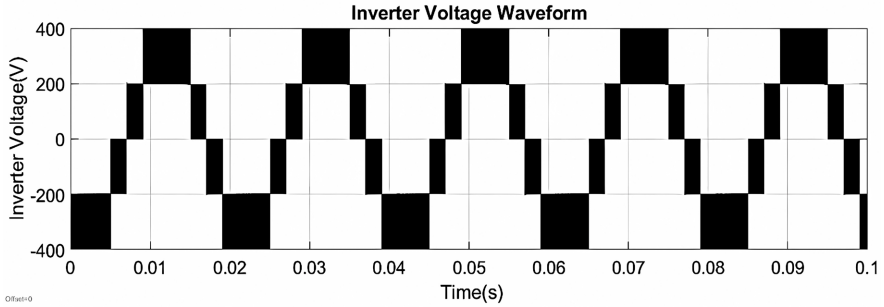


(c)

Figure 7. Inverter output voltage for (a) two-level inverter (b) three-level inverter (c) five-level TCHB inverter.

Figure 8 shows the FFT analysis result for the five-level TCHB inverter voltage waveform without a filter. The voltage THD is equal to 36.35% when the amplitude modulation ratio is 0.85. The harmonic spectrum is efficiently shifted by the high switching frequency, which lowers the filter size needed for sufficient ripple attenuation. The graphs of inverter output voltage THD in relation to the amplitude modulation ratio for the two-level, three-level, and five-level inverters without a filter are depicted in Figure 9. The results indicate that the evaluated five-level TCHB inverter demonstrates a reduced THD. As the number of levels increases, the THD decreases, indicating enhancement in the quality of the inverter

output waveform.

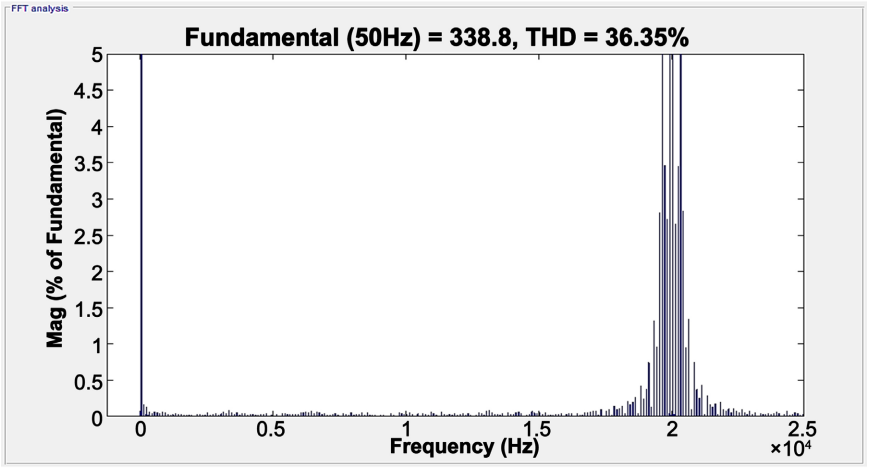


Figure 8. FFT analysis result of five-level TCHB inverter voltage waveform for $M_a = 0.85$.

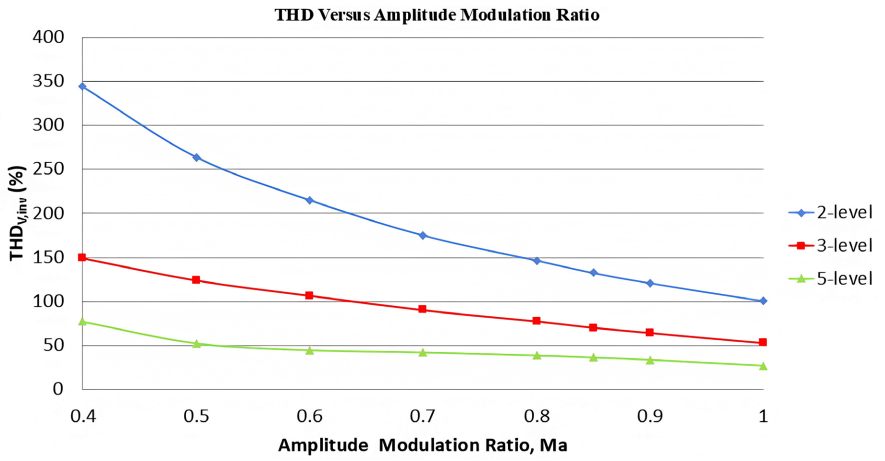
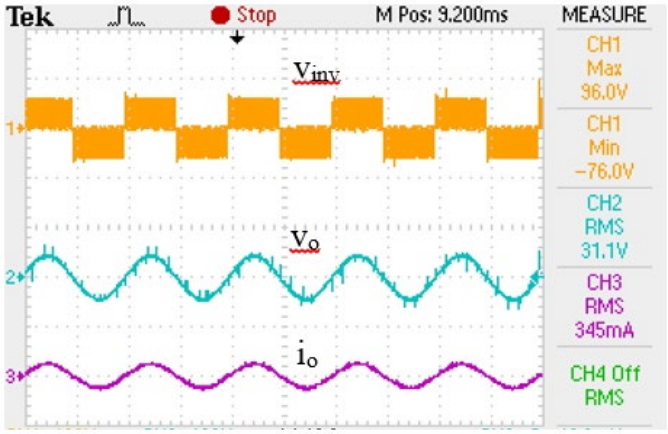


Figure 9. THD versus amplitude modulation ratio of two-level, three-level and five-level inverters without filter.

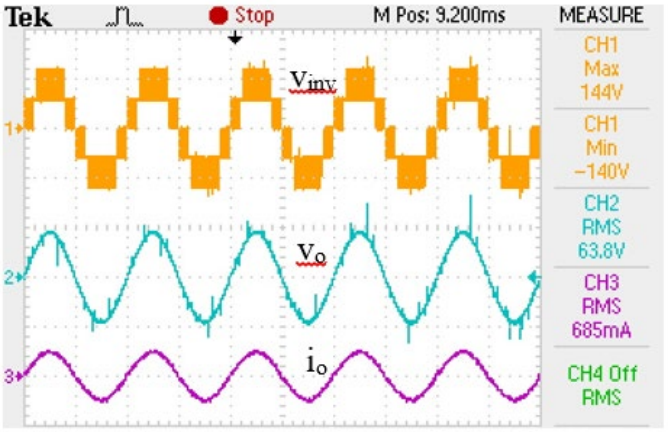
4.2. Hardware Results

The single-phase five-level TCHB inverter hardware is developed and constructed for hardware analysis. In order to obtain sinusoidal output voltage in the adopted multilevel inverter appropriate filter, switching frequency, and control strategy must be selected. The closed-loop control algorithm verification is programmed into the Altera DE2 board and tested on a five-level TCHB inverter prototype to validate the proposed switching scheme. The prototype circuit employs IGBTs of the ultrafast soft recovery diode type (IRG4PC50UD) as switching devices, along with 30CPF12PBF power diodes. The DC bus voltage is set to 120 V. The five-level TCHB inverter with a switching frequency of 20 kHz is set up with an inductive low-pass filter (L_f = 12 mH). The selected inductance, when interfaced with a 100 Ω resistive load, guarantees adequate harmonic suppression and voltage quality, prevents needless voltage loss, and maintains the system's dynamic response.

The five-level TCHB inverter output waveforms are observed when M_a = 0.4 and M_a = 0.8. Figure 10(a) and Figure 10(b) give the experiment results for the unfiltered inverter output and filtered load voltages (v_{inv} and v_o) and the filtered load current (i_o) waveforms for the two mentioned modulation index values. When M_a = 0.4, only three levels of output voltages are obtained for the TCHB inverter circuit, whereas for M_a = 0.8, five levels of output voltages are produced for the TCHB inverter. The filtered load current i_o is in-phase with the filtered load voltage v_o.



(a)



(b)

Figure 10. Inverter output voltage (v_{inv}), filtered load voltage (v_o), and filtered load current (i_o) for: (a) M_a = 0.4; (b) M_a = 0.8.

The experiment results of evaluating for a dynamic change from M_a = 0.4 to M_a = 0.6 and vice versa are presented in Figure 11(a) and Figure 11(b). The filtered load currents i_o are below 5%, while 3.0% and 2.2% THDs are observed when M_a = 0.4 (Figure 12(a)) and M_a = 0.8 (Figure 12(b)), respectively, proving that THD decreases when $0.5 < M_a \leq 1$. The experiment is further extended by testing with various M_a values, resulting total harmonic distortion of the load voltage (THD_v) and load current (THD_i), as illustrated in Figure 13. For the THD_v, it is ranged

between 1.4% and 1.6%, while the THD_i is ranged between 2.2% and 2.6% when $0.5 < M_a \leq 1$. As the M_a increased, both the load voltage and current became more sinusoidal, accompanied by a corresponding reduction in THD.

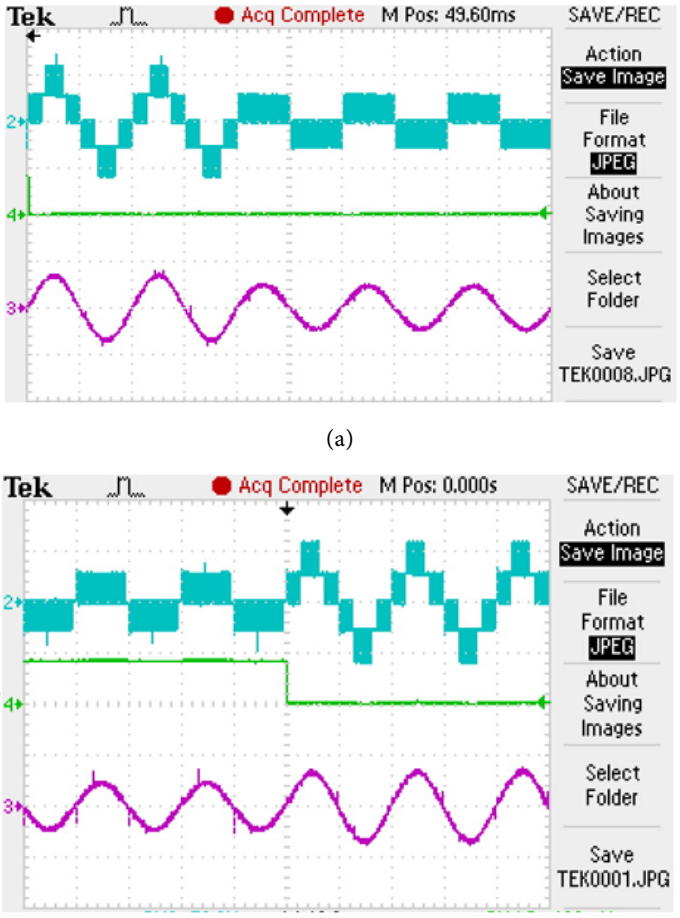


Figure 11. Experiment results: (a) dynamic change of M_a = 0.4 to M_a = 0.6; (b) dynamic change of M_a = 0.6 to M_a = 0.4.

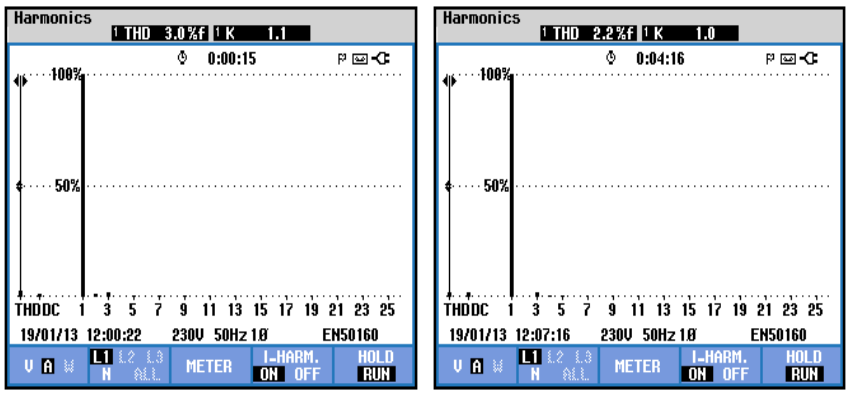


Figure 12. THD of filtered load current i_o at: (a) M_a = 0.4; (b) M_a = 0.8.

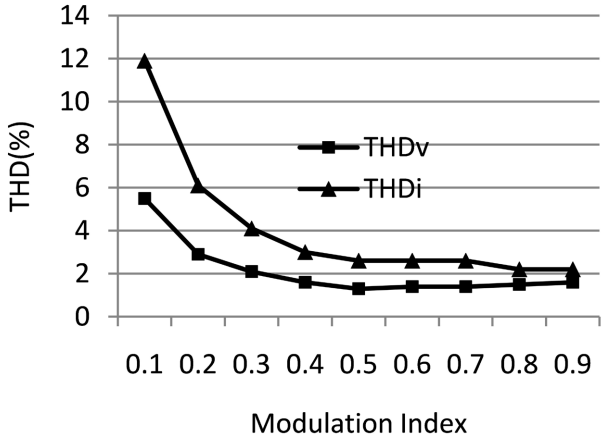


Figure 13. THD_v and THD_i against various modulation indices.

5. Conclusion

This paper presents the design and implementation of a single-phase five-level TCHB inverter using FPGA. This topology uses a multicarrier PWM technique consisting of two carrier signals and one reference signal to generate the PWM switching signal. The simulation results show that the THD decreases when the number of inverter levels increase; thus, the proposed five-level inverter is better than two-level and three-level inverters. By integrating a suitable filter, operating at an appropriate switching frequency, and applying an effective control strategy, the adopted inverter produces sinusoidal output voltage and current. Additionally, using only an inductive low-pass filter, the overall THD for both load voltage and load current waveforms remains below 3% for modulation indices in the range of $0.5 < M_a \leq 1$. When the amplitude modulation ratio is set to be less than or equal to 0.5, the proposed inverter will act like a three-level inverter.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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