

Design of a 14-Bit 1 MS/s Successive Approximation Analog-to-Digital Converter

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How to cite this paper: Li, Q.H., Cao, X.G., Wang, L.B. and Song, M.J. (2024) Design of a 14-Bit 1 MS/s Successive Approximation Analog-to-Digital Converter. *Journal of Power and Energy Engineering*, 12, 59-71. <https://doi.org/10.4236/jpee.2024.1211004>

Received: September 23, 2024

Accepted: November 23, 2024

Published: November 26, 2024

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Abstract

A 14-bit successive approximation analog-to-digital converter (SAR ADC) with capacitive calibration has been designed based on the SMIC 18 μm CMOS process. The overall architecture is in fully differential form to eliminate the effect caused by common mode noise. Meanwhile, the digital-to-analog converter (DAC) is a two-stage structure, which can greatly reduce the area of the capacitor array compared with the traditional DAC structure. The capacitance calibration module is mainly divided into the mismatch voltage acquisition phase and the calibration code backfill phase, which effectively reduces the impact of the DAC mismatch on the accuracy of the SAR ADC. The design of this paper is based on cadence platform simulation verification, simulation results show that when the sampling rate is 1 MS/s, the power supply voltage is 5 V and the reference voltage is 4.096 V, the effective number of bits (ENOB) of the ADC is 13.49 bit, and the signal-to-noise ratio (SNR) is 83.3 dB.

Keywords

Analog-to-Digital Converter, Capacitor Mismatch, Calibration, Successive Approximation

1. Introduction

Digital signals have become the mainstream of modern signal processing due to their excellent ease of storage, ease of transmission, and strong anti-interference ability, and most signal processing work now relies on digital circuits to complete. However, in nature, the signals we come into contact with are analog signals, and in order to convert these analog signals into digital signals for storage and processing, analog-to-digital converters have emerged. With the rapid development of semiconductor processes and integrated circuit technology, the performance of

the analog-to-digital converter has become a key factor in determining the overall effectiveness of the application system.

Currently, there are several mainstream ADC structures: Flash ADC, Pipeline ADC, Sigma-Delta ADC, and SAR ADC, each type of ADC has its own characteristics [1] [2]. Among them, Flash ADCs have faster conversion speeds, usually up to several GHz or more, but their resolution is lower, usually 6 bits or less, and they are mainly used in high-speed digitization processing occasions [3]. Pipeline ADCs work like pipelines, with medium sampling speeds and lower power consumption, but their structures are complex and they have been widely used in the fields of wireless communications, digital video, etc. [4]. Sigma-Delta ADCs have the advantage of being easy to integrate and have a resolution of up to 24 bit, but they have the disadvantage of longer response times and higher power consumption, and are mainly used in audio analysis and measurement [5]. Compared with the above three types of ADCs, SAR ADCs are characterized by low power consumption, high sampling speed, high accuracy, and can be well compatible with nanoscale advanced semiconductor processes, which has become the focus of research in recent years [6]-[8].

A SAR ADC is a highly efficient analog-to-digital converter that uses a binary search algorithm to convert an analog signal into a digital signal, similar to the use of a balance to compare an object of unknown mass with a series of objects of known mass to determine the mass of the unknown object. In a SAR ADC, this process is accomplished using a comparator, a digital-to-analog converter, and a successive approximation register. However, at the current process level, due to factors such as capacitor mismatch, the accuracy of SAR ADCs is limited to a maximum of 12 bits, and 14-bit SAR ADCs must be calibrated using calibration techniques [9]. In this paper, a calibration algorithm is designed to obtain the high-band array error by multiplexing the low-band capacitance array, and the simulation shows that the calibration algorithm reaches the design index.

2. SAR ADC Overall Structure

The SAR ADC structure in this paper is shown in **Figure 1**, which mainly includes the DAC capacitor array, comparator, timing logic circuit, SAR control logic, and calibration part.

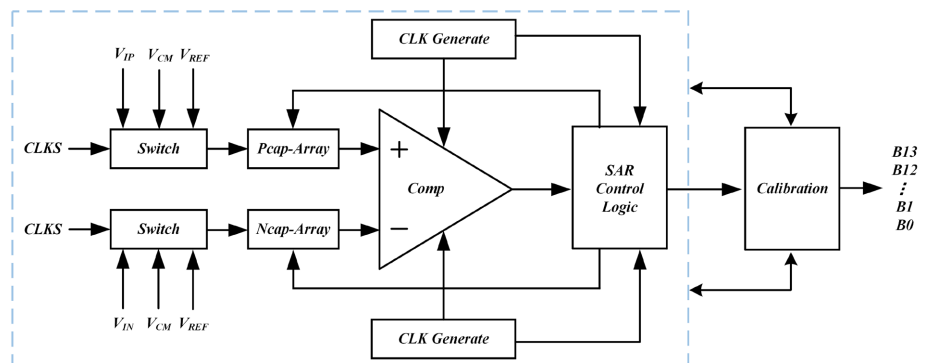


Figure 1. SAR ADC structure.

The overall architecture adopts a fully differential structure, which can effectively suppress common mode noise and improve linearity. Where V_{IP} and V_{IN} are a pair of fully differential input signals, V_{REF} is the reference voltage, V_{CM} is the common-mode voltage, CLKS is the sampling clock, and B13~B0 is the 14-bit digital output code value. During conversion, the differential input signals V_{IP} and V_{IN} are sampled and held by the capacitor array, and then the output sends the obtained effective voltage values to the comparator for comparison, and finally the control logic is responsible for the whole SAR ADC conversion process and generates the correct digital code output. And the calibration module is to correct the accuracy impact caused by the non-binary relationship between the capacitors due to capacitance mismatch. **Figure 2** shows the SAR ADC operation timing diagram, CLKC is the comparator clock, EOC is the end of a conversion signal.

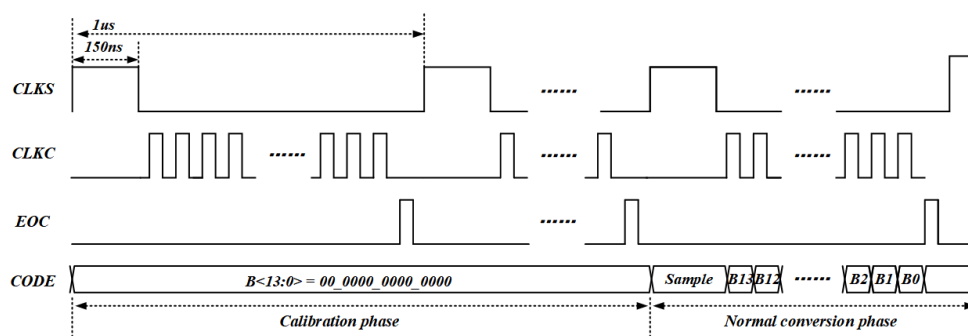


Figure 2. Timing diagram of SAR ADC operation.

2.1. DAC Capacitor Array Design

SAR ADCs can be categorized into current-type, voltage-type, and charge-type structures depending on the structure of the DAC implementation. Due to the continuous maturity of the deep submicron process conditions, the charge-type structure is usually used for realization. The basic principle is to utilize charge conservation and charge redistribution between capacitors to complete the binary successive approximation, which has the advantages of being less susceptible to temperature, higher matching and no static power consumption. In addition, it can integrate the sample-and-hold circuit and capacitor array together, saving the area of the ADC and simplifying the structure of the circuit [10] [11]. Since in a conventional fully binary-weighted capacitor DAC, the number of capacitors in the DAC increases exponentially as the number of ADC bits increases, the number of capacitors required for an N-bit ADC is 2^N , where N is the number of ADC bits. This exponential increase not only leads to a significant increase in hardware cost, but also affects the performance of the DAC. So, in order to minimize the number of capacitors required, segmented capacitor arrays came into existence, first proposed in 1979 by Y.S. Yee *et al.* [12]. The basic idea of segmented capacitor array is to divide the traditional binary weighted capacitor array into multiple smaller subarrays, each subarray is connected with a bridge capacitor, and each subarray has a different weight range, and can be responsible for the conversion of a certain

range of digital codes, the more common is the two-segment structure.

The 14 bit SARADC in this paper is the 8 + 8 segmented structure, as shown in **Figure 3** for the positive end of the DAC capacitor array structure. Since the potential of the lower pole plate of the DAC capacitor array is selected to connect the reference voltage V_{REF} to GND during the conversion phase of the traditional switching timing, while in this paper, the switching timing adopts the VCM-Based timing, in which the potential of the lower pole plate of the DAC is connected from the common-mode voltage V_{CM} to the reference voltage V_{REF+} or V_{REF-} , the switching energy loss is much less than that of the traditional switching timing. The switching energy loss is much smaller than that of conventional switching timing. Secondly, the input signal is sampled by the lower plate, which can effectively avoid the charge transfer caused by parasitic capacitance during sampling and ensure the linearity of the ADC.

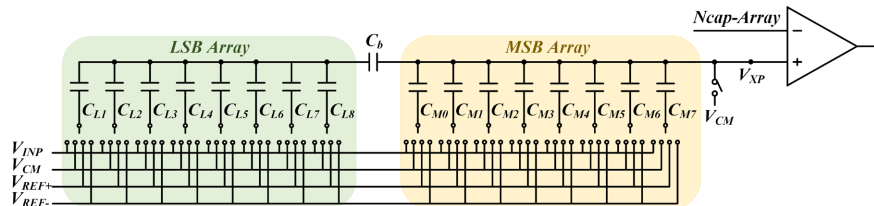


Figure 3. Positive capacitor array structure.

Among them, the high segment capacitance array (MSB) consists of $C_{M0} \sim C_{M7}$, C_{M0} is the compensation capacitance, and the low segment capacitance array (LSB) consists of $C_{L1} \sim C_{L8}$, C_b is the coupling capacitance. Let the capacitance value of the unit capacitor be C_u , then there are:

$$C_b = C_{M0} = C_{M1} = C_{L1} = C_u \tag{1}$$

$$\begin{cases} C_{M(i+1)} = 2C_{Mi} \\ C_{L(i+1)} = 2C_{Li} \end{cases} \quad (i = 1, 2, \dots, 8) \tag{2}$$

First of all, in the sampling stage, the sampling clock CLKS is high, the capacitance array upper plate connected to the common mode level V_{CM} , MSB section lower plate connected to the input signal, while the LSB section lower plate connected to the V_{CM} . when the sampling capacitance is stable, the first disconnect the upper plate, at this time the upper plate is suspended, followed by the lower plate switch from the input signal switching to the V_{CM} , the capacitance array to complete the sampling of input signals and maintain. Then enter the comparison conversion stage, the comparator directly on the capacitor array upper plate voltage comparison, if the comparator result is 1, then $V_{IP} < V_{IN}$, that is, the positive voltage is greater than the negative voltage, control the positive end of the capacitor C_{M7} lower plate connected to the V_{REF+} , the negative end of the C_{M7} connected to the V_{REF-} . Conversely, the positive C_{M7} lower plate connected to V_{REF-} , N-terminal C_{M7} connected to V_{REF+} . When the capacitor array to complete the switch, continue to compare the upper plate voltage and control the capacitor array flip-flop,

one by one to complete the conversion of binary code.

2.2. Unit Capacitor Size Selection

KT/C noise is generated in almost all sampled data systems, and the ADC sampling switch is no exception; this noise is passed to the output after passing through a low-pass filter constructed with an array of capacitors with the noise equation:

$$P_n = \frac{KT}{C_{sample}} \quad (3)$$

where C_{sample} is the total sampling capacitance, K is the Boltzmann constant with a value of 1.380649×10^{-23} J/K. T is the temperature. From Equation (3), it can be seen that the KT/C noise is related to the size of the sampling capacitance, and the larger the capacitance value, the smaller the KT/C noise. Since the KT/C noise in the sampling circuit needs to be much smaller than the quantization noise, and both ends of the DAC are sampled at the same time in this paper, the KT/C noise should satisfy the following equation:

$$2\frac{KT}{C_s} < \frac{\Delta^2}{12} \times \frac{1}{4} = \frac{1}{12} \times \left(\frac{V_{REF}}{2^N}\right)^2 \times \frac{1}{4} \quad (4)$$

When the highest position of the capacitor array switches from 100...00 to 011...11, the worst integral nonlinearity exists in the circuit at this point. To ensure the linearity of the ADC, INL is required to be less than 0.5 *LSB*, according to the 3σ law of normal distribution [13] [14]:

$$\sigma_{INL,MAX} = LSB \frac{\sigma_u}{C_u} \sqrt{2^{N-1}} < \frac{1}{2} LSB \quad (5)$$

$$3\sigma_{INL,MAX} < 0.5 LSB \quad (6)$$

$$\frac{\sigma_u}{C_u} < \frac{1}{6\sqrt{2^{N-1}}} \quad (7)$$

The standard deviation of the unit capacitance value, σ_u , can be obtained by Monte Carlo simulation, and the maximum mismatch rate is 0.1841%. In this paper, the sampling capacitance value is 27.1723 fF ($5 \times 5 \mu\text{m}$), Monte Carlo simulation of the capacitance, the results are shown in **Figure 4**, the capacitance mismatch is normally distributed, the mean value of the unit capacitance size is 27.1724 fF, a standard deviation of 76.8695 aF, the mismatch rate of about 0.2829%, does not satisfy the static performance of the 14-bit SAR ADC, so it is necessary to use a calibration algorithm to calibrate the capacitance mismatch. Therefore, a calibration algorithm is needed to calibrate the capacitance mismatch. After the calibration algorithm to calibrate the capacitance mismatch verified that the length and width of the MOM capacitor are taken about $5 \mu\text{m}$, can still have good results. 128 units of capacitance in the high segment of the CDAC as a sampling capacitance C_{sample} , the value of about 3.49 pF, which is greater than the minimum value of the KT/C noise required, and thus the sampling thermal noise

on the ADC's impact can be ignored.

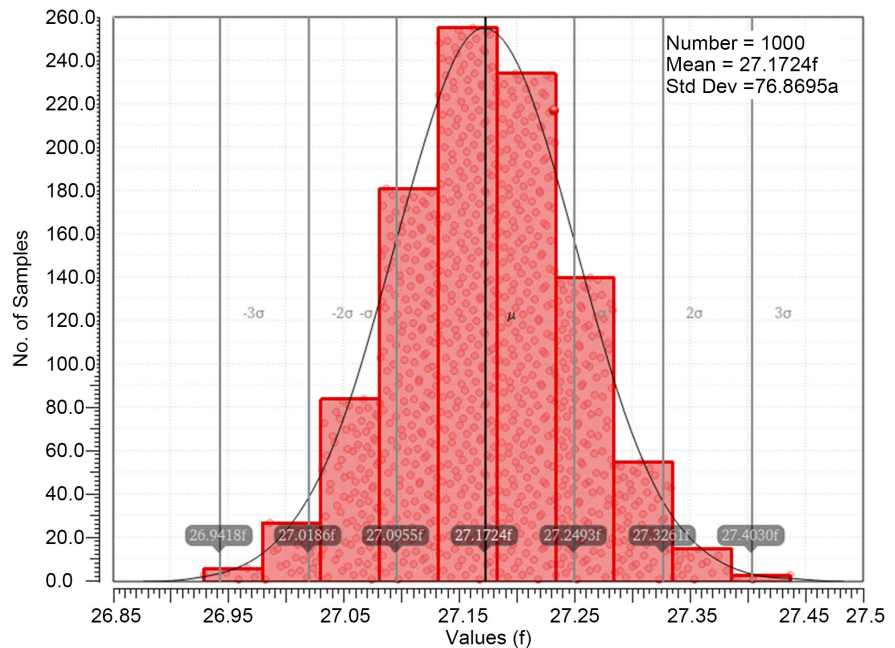


Figure 4. Monte Carlo standard deviation simulation results.

2.3. Sequential Logic Circuit

The control logic of the SAR ADC is divided into two kinds of synchronous timing and asynchronous timing, when the sampling clock frequency is not high, synchronous timing has the characteristics of stable timing and low power consumption, so this paper adopts synchronous timing logic circuits, as shown in Figure 5 and Figure 6 for the schematic and timing diagrams, respectively. CLKS is the sampling clock, Valid is the flag signal for the comparator to complete a comparison, and Clk<15:0> is the synchronous logic clock signal generated by the cascade flip-flop. Start sampling, valid is high, this time the shift register array in the reset state, Clk<15:0> output is 000...00. When the end of sampling, and the comparator to complete the first comparison, because the first flip-flop input access VDD, this time in the role of the flag signal, the clock Clk<15> to generate a high level, used as a switch switching circuit control signal. When the comparator completes the second comparison, Clk<15> will be sent to the output through the second flip-flop, at which time Clk<14> generates a high level. And so on, after completing 16 comparisons, Valid goes high, and then another round of sampling output begins.

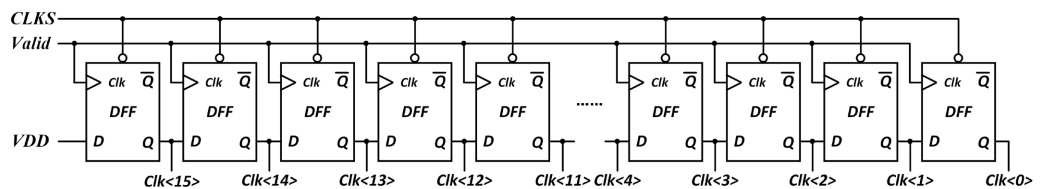


Figure 5. Synchronization timing schematic.

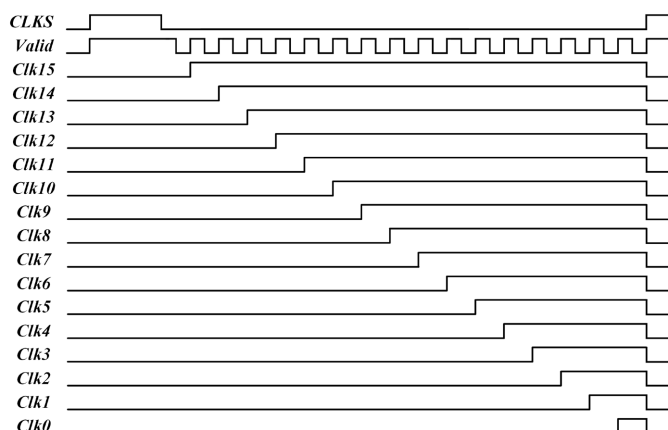


Figure 6. Synchronization timing waveform.

3. Calibration Module Design

Ideally, the parameter dimensions of the capacitor after chip fabrication are exactly the same as the preset values at the time of design. However, in the actual manufacturing process, due to factors such as the edge etching error of the capacitor and the gradient effect of the oxide layer between the upper and lower pole plates of the capacitor, the capacitance value often fails to reach the ideal standard of the design, which triggers the so-called capacitance mismatch problem, capacitance mismatch will affect the ADC's nonlinearity [15]. In this paper, we design an algorithm for mismatch calibration by multiplexing low-segment capacitor arrays, and its basic working principle is as follows: through the different switching of capacitor arrays, we obtain the error voltage of each bit of capacitor in the high-segment capacitor array, and convert the error voltage into an error code value through the progressive approximation logic, and then add the error code value into the capacitor array to control the switch switching during the subsequent normal conversion process to achieve the purpose of capacitance mismatch calibration. Purpose The following is an example of obtaining the highest capacitance mismatch voltage.

Firstly, the upper pole switch of DAC is closed, the highest bit lower pole plate is connected to V_{CM} , the rest of the bit capacitor lower pole plate in the positive MSB is connected to V_{REF+} , the rest of the bit capacitor lower pole plate in the negative MSB is connected to V_{REF-} , and all of the capacitor lower pole plates in the lower section are connected to V_{CM} , at this time, it can be concluded that the amount of charge stored on the capacitance array is Q_1 , and its expression is shown in Equation (8):

$$Q_1 = (V_{CM} - V_{REF}) \sum_{i=0}^6 C_{Mi} \quad (8)$$

Then the capacitor array upper pole plate and V_{cm} disconnect, the positive end of the highest capacitance lower pole plate connected to V_{REF+} , the negative end of the highest capacitance lower pole plate connected to V_{REF-} , all the rest of the capacitance lower pole plate in the DAC are connected to the V_{CM} , at this time, can be obtained on the array of the charge is Q_2 , and its expression is shown in Equation (9):

$$Q_2 = (V_X^{(7)} - V_{CM}) \left(C_{LT} + \sum_{i=0}^6 C_{Mi} \right) + (V_X^{(7)} - V_{REF}) C_{M7} \quad (9)$$

$$C_{LT} = \frac{C_u \sum_{i=1}^8 C_{Li}}{C_u + \sum_{i=1}^8 C_{Li}} \quad (10)$$

Since there is no charge relief loop in the capacitor array before and after switching, it is known from the charge conservation theorem that $Q_1 = Q_2$, which is solved for:

$$V_X^{(7)} = V_{CM} \quad (11)$$

From Equation (11), the voltage at the output of the DAC before and after the conversion is then equal to V_{CM} , however, when there is a mismatch in the capacitor, the voltage at the output of the DAC should be the sum of V_{CM} and a mismatch voltage:

$$V_X = V_{CM} + \frac{C_{M7} - \sum_{i=0}^6 C_{Mi}}{C_{total}} V_{REF} = V_{CM} + \epsilon_N V_{REF} \quad (12)$$

The mismatch voltage caused by the highest bit at this point is:

$$V_{mis}^{(M7)} = \frac{C_{M7} - \sum_{i=0}^6 C_{Mi}}{C_{total}} V_{REF} \quad (13)$$

Therefore, as long as the capacitance of the DAC is determined, the mismatch voltage for each bit can be obtained according to the above method. A timing diagram of the high seven-bit capacitance error is shown in **Figure 7**.

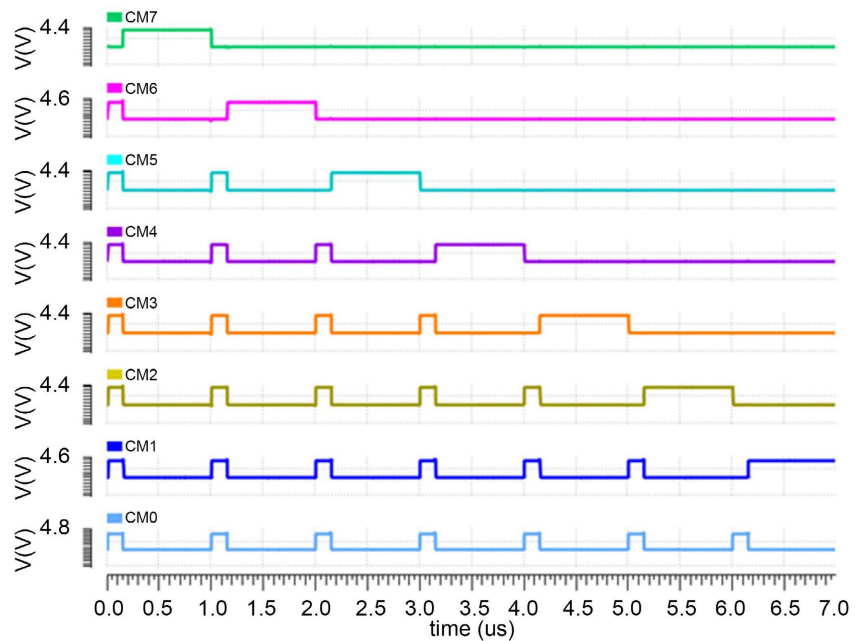


Figure 7. Timing sequence of the calibration process.

After the previous stage, the error voltage has been extracted and stored in the output of the DAC capacitor array, the next step is to use the low capacitance of the DAC capacitor array to quantise the error voltage, generating a 9-bit error code $D_{mis}^{(7)}$, which is similar to a 9-bit fully differential successive approximation analogue-to-digital converter conversion process. Finally, during normal ADC conversion, the resulting error code is used to control the capacitor array conversion. However, in the normal conversion process back to complement the error code, the value of the high bit is determined to be 1 or 0, will have an impact on the normal conversion of the next bit of capacitance, therefore, in the normal conversion process used in the actual code value is not $D_{mis}^{(7)}$, but the calibration code value $D_{cal}^{(7)}$, where:

$$D_{cal}^{(7)} = \frac{1}{2} D_{mis}^{(7)} \quad (14)$$

Similarly, the following relationship exists for the remaining 6-bit capacitance calibration code values of the MSB:

$$D_{cal}^{(i)} = \frac{1}{2} \left(D_{mis}^{(i)} - \sum_{j=i+1}^6 D_{cal}^{(j)} \right) \quad i = 1, 2, \dots, 6 \quad (15)$$

Simulation

The SAR ADC calibration algorithm was first validated based on the SMIC. 18 μm BCD process. Set under the conditions of sampling frequency of 1 MHz, input signal frequency of 303 K and process angle of TT, respectively, the:

- 1) without mismatch.
- 2) with mismatch without calibration.
- 3) with mismatch with calibration.

Three cases using the Cadence platform for simulation, the ADC output of 14-bit digital code word through the ideal DAC reduction and fast fourier transform can be obtained:

- 1) Without mismatch, ENOB = 13.93 bit, SNR = 85.66 dB.
- 2) With mismatch without calibration, ENOB = 8.89 bit, SNR = 55.3 dB.
- 3) With mismatch and calibration, ENOB = 13.49 bit, SNR = 83.3 dB.

The results are shown in **Figures 8-10**, respectively. It can be seen that after adding the calibration algorithm, the ENOB of the SAR ADC is improved by 4.65 bit and the SNR is improved by 28 dB, and the calibration effect is obvious.

Secondly the SAR ADC process angles are simulated and the results are shown in **Figure 11**, **Figure 12** respectively. ENOB = 13.47 bit and SNR = 82.87 dB for SAR ADC at FF process angle and ENOB = 13.43 bit and SNR = 82.67 dB at SS process angle. It can be seen that there is little difference in performance between the process corners.

Finally, the power consumption of the overall SAR ADC circuit is verified, and the simulation shows that the overall power consumption of the ADC is 6.93 mW.

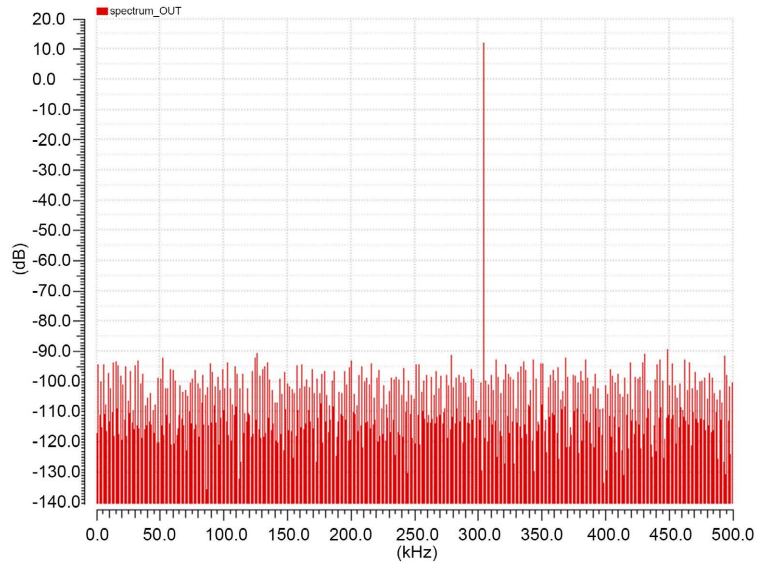


Figure 8. Without mismatch.

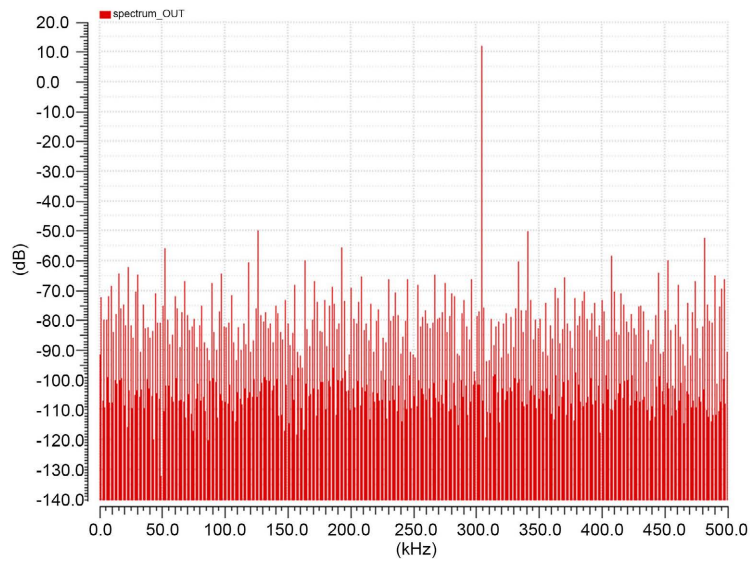


Figure 9. With mismatch without calibration.

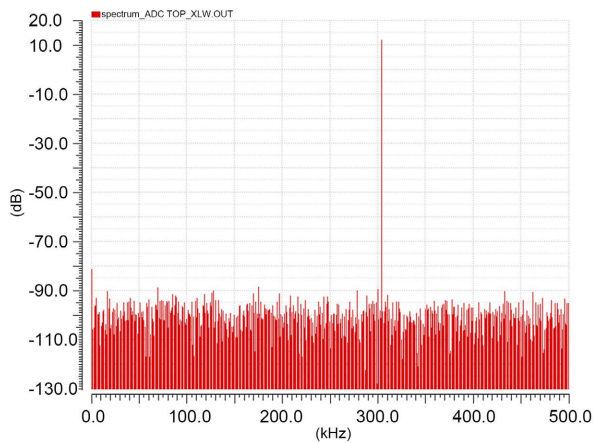


Figure 10. With mismatch and calibration.

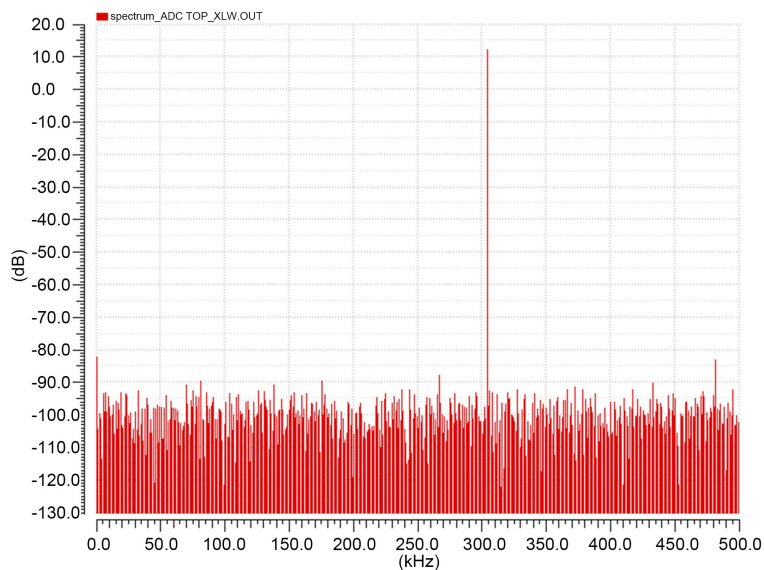


Figure 11. FF corner.

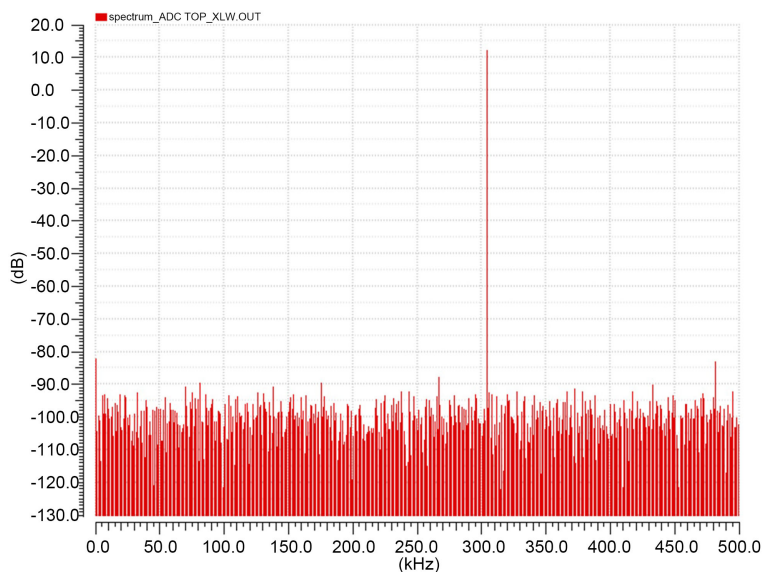


Figure 12. SS corner.

4. Conclusion

Firstly, based on the SMIC. 18 μm BCD process, this paper designs a 14 bit 1 MS/s fully differential SAR ADC with capacitive mismatch calibration, in which the capacitive array adopts the fully differential form, which can effectively improve the common-mode rejection capability. The calibration algorithm calibrates the high segment by multiplexing the low segment capacitance array, and since the low segment mismatch has less effect on the accuracy, the low segment can be calibrated without calibration to achieve higher accuracy. Secondly, the simulation results show that after adding the calibration, the effective bit number of the SAR ADC is increased from 8.89 bit to 13.49 bit, and the SNR is increased from 55.3 dB to 83.3 dB, which is a great improvement of its performance parameters.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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