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Design and Implement of Low Power Consumption SRAM Based on Single Port Sense Amplifier in 65 nm

Shunrui Li, Jianjun Chen, Zuocheng Xing, Jinjin Shao, Xi Peng

Collage of Computer Science of National University of Defense Technology, Changsha, China
Email: lisr824467100@163.com, cjj192000@163.com

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Abstract

With the rapid development of integrated circuits [1], low power consumption has become a constant pursuiting goal of the designer in chip design. As the memory almost takes up the area of the chip, reducing memory power consumption will significantly reduce the overall power consumption of the chip; according to ISSCC's 2014 report about technology trends discussions, there two points of the super-low power SRAM design: 1) design a more effective static and dynamic power control circuit for each key module of SRAM; 2) ensure that in the case of the very low VDD min, SRAM can operating reliably and stably. This paper makes full use reliable of 8T cell, and the single-port sense amplifier has solved problems in the traditional 8T cell structure, making the new structure of the memory at a greater depth still maintain good performance and lower power consumption. Compared with the designed SRAM the SRAM generated by commercial compiler, as the performance loss at SS corner does not exceed 10%, the whole power consumption could be reduced by 54.2%, which can achieve a very good effect of low-power design.

Keywords

Single Port Sense Amplifier, SRAM Design, Low Power Design, 8T SRAM

1. Introduction

For dynamic power consumption, the most effective way to reduce power is the use of very low power supply voltage, for the relationship between the power consumption and the supply voltage is: the power consumption is proportional to the square of the supply voltage; for static power consumption, the low-voltage design techniques also is the most direct and effective way, because leakage power will be low enough when SRAM power supply voltage is low enough.

In this thesis, based on a 65 nm process single-port sense amplifier, designed an 8T_SRAM circuit, and compared this SRAM with the generated SRAM by memory compiler in performance, on the premise of speed quite, the former has much more advantage in power and stability.

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2. Entire Circuit Structure

Full custom SRAM 512 × 32 memory structure is composed of 8T_SRAM. The circuit structure is shown in **Figure 1**. The whole circuit is divided to five parts, such as clock, latch, decoder, storage arrays and IO. The use of single port IO sense amplifier circuit in this paper, making this new SRAM acquire lower power consumption, higher performance and higher reliability compared with the conventional circuit configuration.

The key of SRAM circuit design is the reading circuit, because the performance of the read circuit determines the reading speed of the SRAM, and the read circuit is the critical path in the SRAM, so reducing the delay on the critical path can effectively improve the timing performance of memory.

2.1. Bit Cell

Due to the characteristics of 6-T SRAM [2] memory's structure, the data output are all using double-port sense amplifier to detect bit line voltage difference, and amplified voltage difference to output. But with the process size reduction and lower power supply voltage, the stability of the 6-T cell is getting worse, more and more weak of noise immunity, noise margin getting smaller and smaller, so it is difficult for sense amplifier circuit to control the time of turning on and off, and the worst is there often rise a noise voltage turning up on the bit line, and amplified by sense amplifier to output which results in erroneous operation. The design of the SRAM structure proposed in this paper is using 8-T cell, because of its better stability than6-T, 8T is a big trend of future development. Although compared with 6-T cell, 8-T cell has another two transfer transistors, the transistor size is not limited to read without breaking the rules and can follow the minimum rules to design, and 8T cell area below 65 nm process can be done fairly compared with 6T cell area, so the 8T_cell area does not increase. 8T_cell structure is as follows **Figure 2**.

2.2. Sense Amplifier IO Block

Traditional 8T memory cell read operation use single-port sense amplifier, and the conventional domino logic single-port sense amplifier circuit just uses this sense amplifier. Domino circuit structure is shown as **Figure 3**.

Domino sense amplifier logic circuit is the most typical one of those single-port sense amplifier circuits, and is also the most common single- port sense amplifier logic. Though this single-port sense amplifier logic in the small SRAM has a good performance, with the increase of cell number on the bit line RBL, the performance and power consumption will be a sharp deterioration. That is because as the mount too many cells, the RBL load

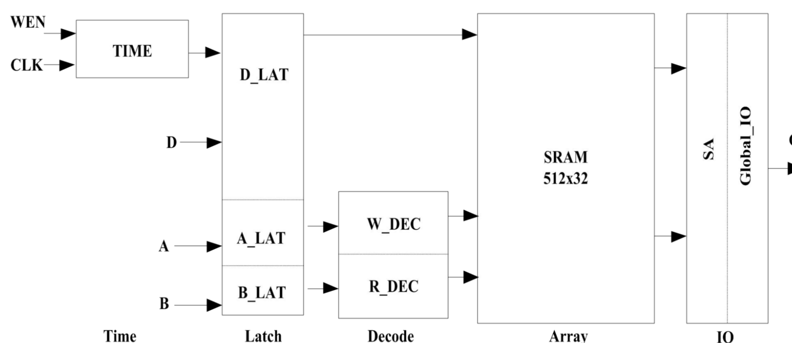


Figure 1. SRAM circuit configuration.

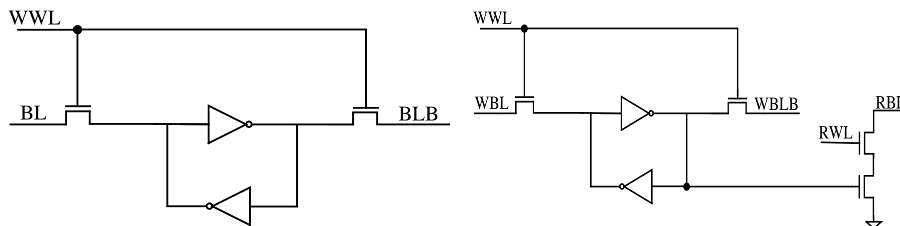


Figure 2. 6-T cell and 8-T cell circuit.

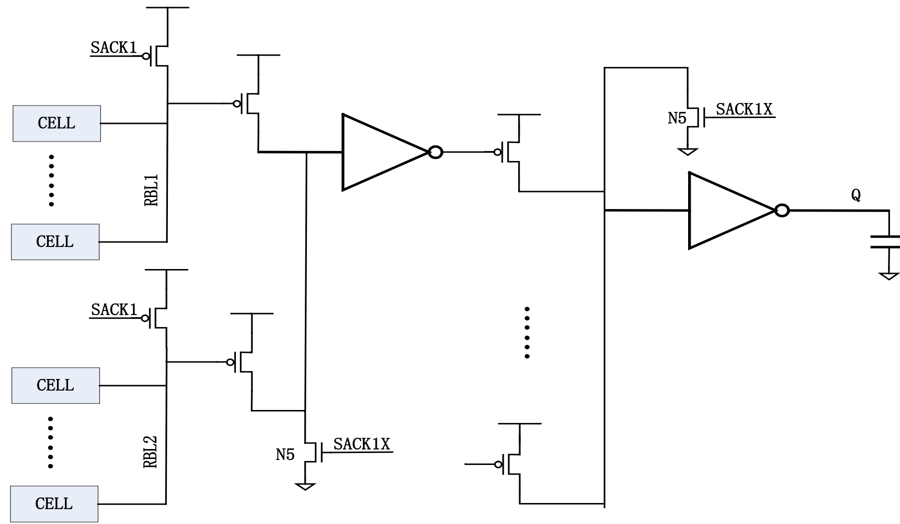


Figure 3. Domino logic circuit diagram.

capacitance is too big, the pre-charge time is longer, and the discharge time is also longer. Additionally, the single-port sense amplifier logic bit line voltage is full swing between 0-VDD, each discharge will have a great dynamic power. Therefore, power consumption also seriously deteriorated.

Based on those drawbacks of the single-port sense amplifier, TBP (Trip point Bit-line) solves this kind of problems better, make the sense amplifier remains high performance and can keep very low power consumption in condition of the high capacity and a long bit line load. **Figure 4** is TBP-sensitive amplifier circuit [3] structure.

Firstly introduce about the structure of the sensitive amplifier circuit. This sensitive amplifier circuit is a single port sense amplifier, which in the sense amplifier module is made up of a static complementary inverter INV, a balance PMOS transfer P3, a transmission gate T, the NMOS transistor N3 and a precharge transistor N1. Among those components, the inverter, in which the pull-down network of it is controlled by the enable signal REN. This can effectively reduce the static leakage current of the sensitive amplifier. So the read enable signal of the sensitive amplifier is effective. At the rest of the time, REN = 0 the sense amplifier doesn't work, N3 and N2 can form the DIBL effect which can reduce the static leakage current.

The TBP sensing scheme is to directly precharge RBL to the trip point of the inverter INV. During the precharge phase, the SACK1 turns on the precharge NMOS transistor N1and N5, for charging RBL and Z respectively. At the same time, transmission gate T is turned on, and the INV input, LBL, is connected to the output Y. This precharges LBL near the trip-point of the sense amplifier by the precharge NMOS transistor N1 and the diode-connected PMOS transistor P1, and thus, the offset of the sense amplifier is compensated. The working process of the sensitive amplifier is also divided into two stages, the pre-charge stage (SACK1 = 1) and the evaluation phase (SACK1 = 0).

When reading 0, supposed that the value 0 will appeared on the RBL1, then the bit line RBL1 will discharging, due to the bit line voltage value is at the trip-point of the inverter, so the voltage gain is very big at this point. When the bit line voltage drops, then P3 MOSFET opens, the output voltage of Y point is quickly pulled high, Z point is pulled high, then output GRBL = 0, and P2 is turned on at the same time, making the voltage of Z pulled up faster to the steady high level state. P2 formed a positive feedback circuit [4], which can make the sense amplifier speed up. When reading 1, it will be auto-zero [5], the voltage of bit line will not drop, the voltage of the X point will not up or down, so the voltage of the Y point will not drop, P3 will not open, the voltage of Z point will remain low, outputs GRBL = 1, the feedback circuit is closed. This is calling regenerative sensing logical [6]. The operational waveforms of the TBP sensing scheme are shown in **Figure 5**.

3. Results Contrast

The data on the **Table 1** and **Table 2** shows the sensitive single-port amplifier circuit performance and memory compiler SRAM and tradition in the case of a considerable delay, power consumption was greatly reduced,

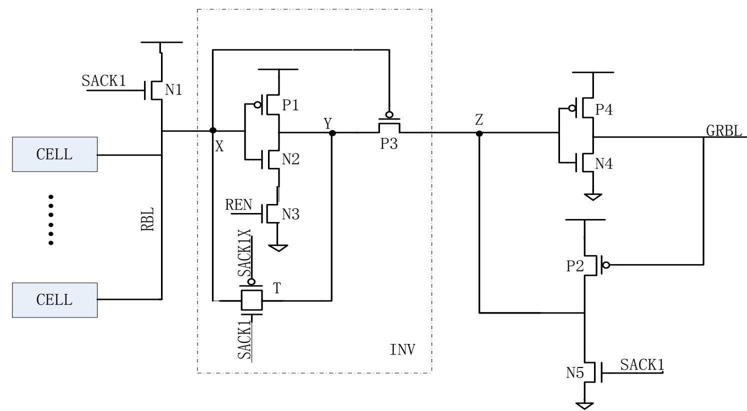
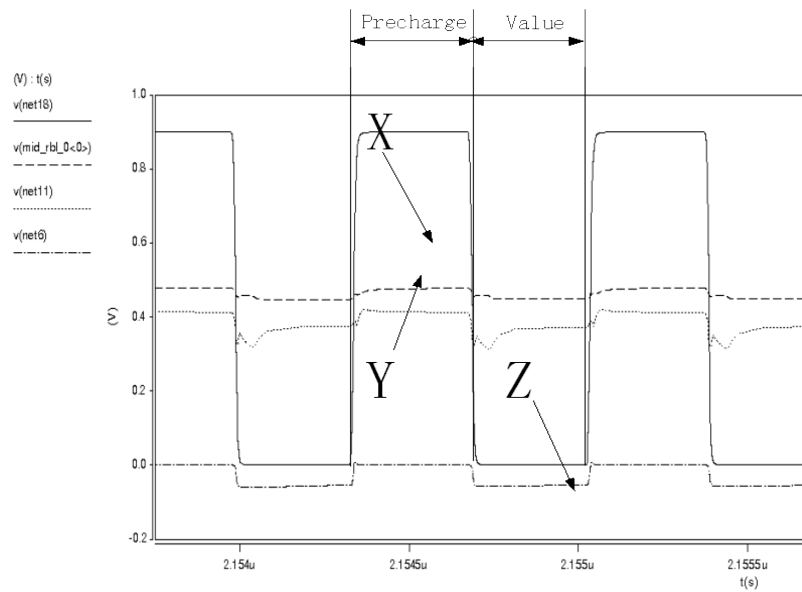


Figure 4. TBP-sensitive amplifier circuit structure.



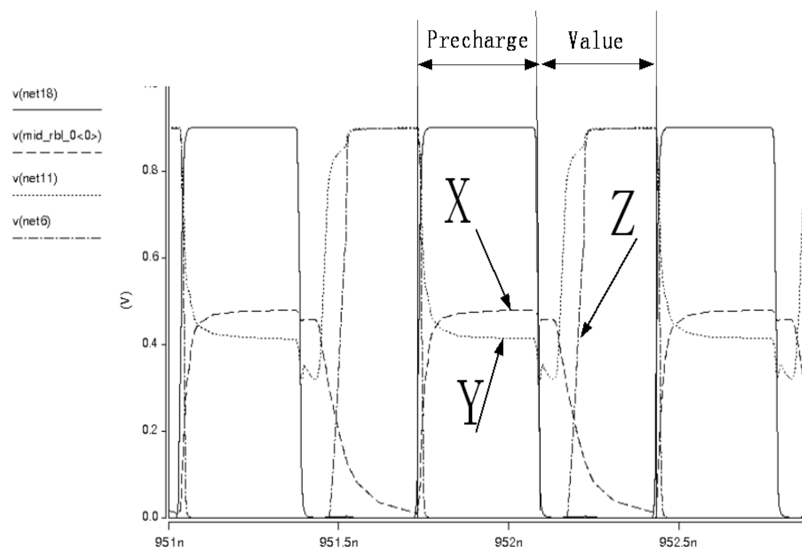


Figure 5. The waveform of sensitive amplifier read 0 and read 1.

Table 1. Dynamic power.

Power consumption	Compiler SRAM (W)	TBP-Sense-amplifier SRAM (W)	Percentage
SS corner	8.1e−3	3.85e−3	−52.4%
TT corner	1.3e−2	7.03e−3	−45.9%
FF corner	1.55e−2	1.16e−2	−25.2%

Table 2. CLK-Q_delay.

CLK-Q	Compiler SRAM (ns)	TBP-Sense-amplifier SRAM (ns)	Percentage
SS corner	0.694	0.768	+9.01%
TT corner	0.477	0.505	+5.82%
FF corner	0.291	0.316	+8.6%

which reduces power consumption at FF corner (25.2%), the TT corner under power reduction (45.9%), at SS corner reduce power consumption (52.4%). Because sensitive single-port amplifier circuit is reduced by 50% of the bit line voltage swing, additional use of decoding module, reducing the length of the bit line, and can be decoded by the address block, reducing unnecessary decoding circuit higher over so decoding module efficiency, dramatically reducing the overall power consumption of SRAM.

4. Summary

This paper finished a 512 × 32 SRAM circuit design; the aim was highly reliable, high speed, and low power consumption design, and separately with the commercial compiler SRAM performance comparison by circuit design and verification. At an equal speed, power consumption was lower than memory compiler SRAM. It shows that this design has achieved satisfactory results; the full-custom design of SRAM is very successful. Some good design methods were also proposed; it was worth to be used in other reference full-custom design.

Acknowledgements

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