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Digital biomedical electrical impedance tomography based on FPGA

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ABSTRACT

A digital biomedical electrical impedance tomography (EIT) system is developed with the aid of FPGA. The key elements of EIT system are described specifically in the paper. The functions are realized to generate excitation source, switch electrode channels, deal collected signals, demodulate measured voltages etc. The system is tested by a circular tank with 16 stainless electrodes attached around the boundary. The adjacent incentive adjacent measurement mode is adapted to collect boundary voltages of the interesting field. By testing, the system works with 36 dB signal-to-noise ratio (SNR) when 1 mA 100 KHz current is applied into a homogenous tank.

Keywords: Electrical Impedance Tomography; FPGA; Direct Digital Synthesis; Orthogonal Sequences Demodulation

1. INTRODUCTION

Electrical impedance tomography (EIT) is one of the major research topics in biomedical engineering. It is a medical imaging technology developed in thirty years after morphological and structure imaging technology. EIT system consists of the electrode array, data acquisition system (DAS) and image reconstruction. DAS transfers the measured electrical data to computer for subsequent reconstruction. The quality of the reconstructed image depends on the accuracy of the collected data and the reconstruction algorithms mostly. Therefore, it is essential to design a stable and accuracy DAS for EIT system.

At the beginning of the research, around 1980s, the electrical processor are not as powerful and integrated as now, microprocessor is taken the charge of coordinating the whole system. Mark I and Mark II established by Sheffield University are the examples [1,2]. With the development of the digital processing technology, DSP became the most popular processor used in EIT system for a certain long time. Mark3a and Mark3b [3], OXBACT 3 and 4 [4], ACT3 [5] and Dartmouth EIT system [6] are the representatives. In OXBACT system, Oxford Brookes University used TMS320C40 as the controller; Dartmouth researchers used ADSP-21065L to build their multi-frequencies EIT system. These systems worked well and made great contribution to EIT research.

FPGA is one of the most popular electric circuit design methods at present, which is developed on the basis of PAL and GAL, and has the advantages of high performance, big scale integration, programmable ability. In recent years, some Chinese research groups have used FPGA to develop EIT system, such as, Tianjin University used FPGA to construct a EIT system for lung ventilation monitoring [7]; Zhengzhou University used FPGA embedded NIOS II processor to develop a 128 electrodes rotating EIT data acquisition system [8]; the Fourth Military Medical University developed a FPGA EIS system to image the human brain [9].

From the developing view, the digital integrated DAS will bring great promotion to improve EIT clinical applications.

In this paper, XC3S500E-5FG320 of Spartan3E is used as the core controller to implement DAS, which has a large number of resources in FPGA, so it is easy to realize various hardware modules by VHDL (Very high speed integrated circuit Hardware Description Language), which can reduce PCB areas, save development time, and improve the reliability of the system. The cored elements of the DAS are described specifically as following.

2. STRUCTURE

The DAS includes six components: excitation source, switches, signal processing circuits, orthogonal sequences demodulation, data buffer and communication interface, as shown in **Figure 1**. The PicoBlaze microcontroller embedded in FPGA coordinates the parts work effectively [10].

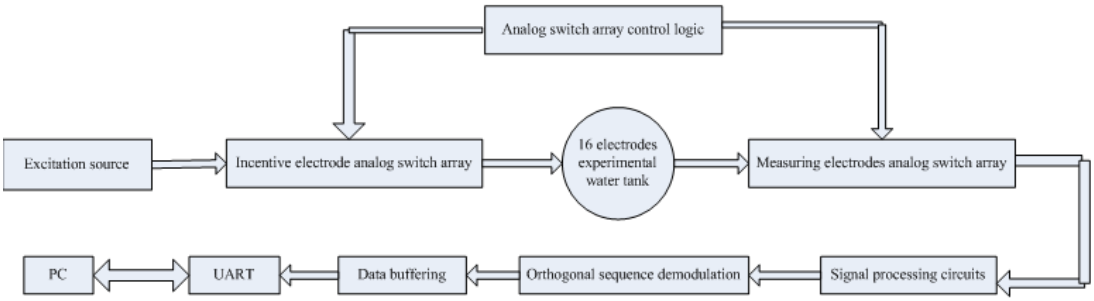

Figure 1. DAS principle figure.

The working process of the system can be described as following.

A sine current signal with small amplitude and fixed frequency is applied to a pair of electrodes. The differential voltages on the other neighboring electrodes are collected in sequence. Each measured voltage is amplified and filtered through the signal processing circuits firstly. Then, the voltages are converted to 14 bits digital signals by analog-to-digital converter AD9240 secondly. Through orthogonal sequence demodulation, the real and imaginary parts of the measured voltages are acquired and sent to reconstruction computer for imaging finally. As adjacent incentive measure working mode is used, the measured voltages are 208. The excitation electrodes and the measured electrodes are chosen by multiplexed switches controlled by FPGA.

3. HARDWARE DESIGN

3.1. Clock Distribution

The precision of the clock is very important for a high-speed digital system, which determines work status and accuracy. There are three digital clock manager (DCM) modules integrated in XC3S500E outputting 50 MHz, 5 MHz and 125 MHz pulse signals respectively. 50 MHz signal is set to be the FPGA working clock; 5 MHz clock signal is connected to AD9240, as a sampling clock signal; 125 MHz clock signal is connected to AD9754, as a digital-to-analog conversion clock signal.

3.2. Excitation Source

In order to meet the requirements of stability, accuracy, dynamic range and signal-to-noise ratio of excitation source, direct digital synthesis technology (DDS) is used to achieve a programmable excitation source [11]. DDS module is built by DDS compiler in IP core. The frequency and the phase of the excitation current are determined by two different control words separately, *PINC* and *POFF*. Phase incremental control word *PINC* and phase offset control word *POFF* are both set in DDS compiler. The frequency is determined by

$$PINC = \Delta\theta = 2^{B_{g(n)}} \times \frac{f_{out}}{f_{clk}} \quad (1)$$

where, $B_{g(n)}$ is the width of phase accumulator, f_{out} is the output frequency and f_{clk} is the clock frequency.

The *POFF* word is related to the starting phase, is decided by

$$POFF = 2^{B_{g(n)}} \times \frac{\varphi}{2\pi} \quad (2)$$

where, φ is the initial phase. The phase can be adjusted continuously by *POFF*.

In this design, the frequency of excitation source is 100 KHz, *PINC* is 0068DB8BH, no spurious dynamic range is 80 dB, and the frequency resolution is 0.0234 Hz.

The digital voltage signal is converted into analog signal by high-speed digital-to-analog converter AD9754, and filtered by second-order Butterworth low-pass filter circuits composed by AD8066. After that, a periodic sinusoidal analog voltage signal is generated.

Under the medical application, safe current excitation (amplitude is less than 5 mA) is taken into design. The voltage signal is turned into safe current signal through the voltage-control-current source (VCCS) module, which is realized by improved Howland circuit composed by AD8021, as shown in **Figure 2**. In the design, 1 mA 100 kHz safe current is achieved.

3.3. Analog Switch Array and Logic Control

Four pieces of analog switch chips MAX4598 are used to choose incentive electrodes, due to its 45 Ω on-resistance, 1 Ω resistance between channels, −80 dB @ 1 MHz, crosstalk between channels, and −90 dB @ 1 MHz off-isolation. An analog switch array chip MT8816 is adopted to select the measured electrodes, as of its small distortion, wide switching bandwidth, and small on-resistance. This strategy can reduce complexity and instability of circuit, and improve the reliability of system as well as the consistency of various channels. In order to save IO ports of FPGA, four data-buffering chips 74HC574 are used as buffers.

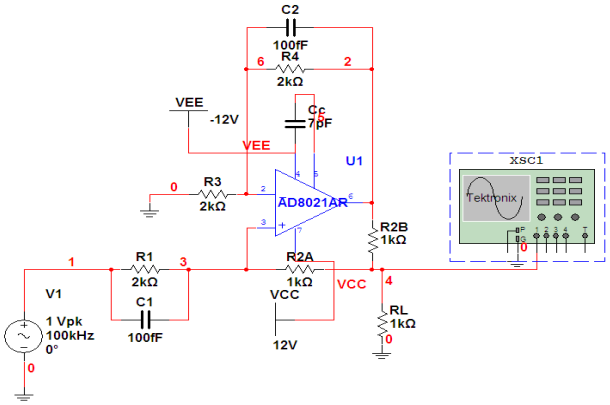

Figure 2. Improved Howland circuit.

3.4. Signal Processing Circuit

The signal processing circuit includes three parts: filtration, amplification, and analog-to-digital conversion. The structure of signal processing circuits is shown in **Figure 3**. Considering the weakness of the signal, twice amplifications are applied. As common disturbances are existed in the measured voltages, differential amplification is adopted firstly. AD8130 is a differential amplifier with high common mode rejection ratio at high frequency and high input impedance. The second amplification is completed by a programmable gain amplifier THS7001. The amplified times are set by PicoBlaze. There is a second-order low-pass filter in THS7001 also. The filtered signal is sent to an analog-to-digital converter AD9240 with 14 bits precision.

3.5. Orthogonal Sequences Demodulation and UART

To take full advantages of FPGA, orthogonal sequence demodulation method is used to overcome the disadvantages appeared in analog demodulation [12]. This strategy can save time, improve reliability. When DDS generates a sine excitation signal, another cosine reference signal is achieved at the same time with the same frequency, which ensures the reference signal has the same characteristics with the excitation signal and guarantees the demodulation accuracy. The orthogonal sequence demodulation is illustrated in **Figure 4**.

The sine signal and cosine signal of the DDS are respectively multiplied and accumulated by MAC. The real and imaginary parts of the voltages are calculated as formulae (3)-(7).

$$u(n) = A\cos\left(\frac{2\pi}{N}n + \theta\right) \tag{3}$$

$$r(n) = \cos\left(\frac{2\pi}{N}n\right) \tag{4}$$

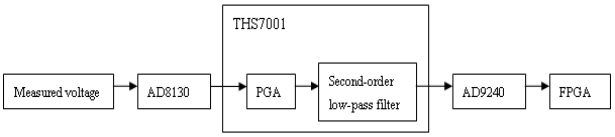

Figure 3. Principle of signal processing circuit.

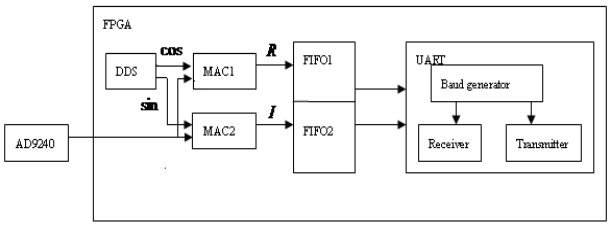

Figure 4. Principle of orthogonal sequences demodulation.

$$q(n) = \sin\left(\frac{2\pi}{N}n\right) \tag{5}$$

$$\begin{aligned} R &= \sum_{n=0}^{N-1} r(n)u(n) \\ &= \sum_{n=0}^{N-1} \cos\left(\frac{2\pi}{N}n\right) A\cos\left(\frac{2\pi}{N}n + \theta\right) \\ &= \frac{1}{2}NA\cos\theta \end{aligned} \tag{6}$$

$$\begin{aligned} I &= \sum_{n=0}^{N-1} q(n)u(n) \\ &= \sum_{n=0}^{N-1} \sin\left(\frac{2\pi}{N}n\right) A\cos\left(\frac{2\pi}{N}n + \theta\right) \\ &= \frac{1}{2}NA\sin\theta \end{aligned} \tag{7}$$

where, $u(n)$ is measured signal; $r(n)$ is reference signal; $q(n)$ is orthogonal reference signal. θ is a phase shift caused by medium or circuit; N is the sampling points. In this design, N is set to 300. Namely, demodulation will be executed after each voltage is sampled 300 times. The range of n is from 0 to $N-1$. R is the real part matrix of the voltage, and I is the imaginary matrix of the voltage.

After orthogonal sequences demodulation, real part and imaginary part are respectively stored in FIFO1 and FIFO2, which are two asynchronous first-in first-out (FIFO) memories with 256 written depths, 32-bit written width, 1024 read depth, 8-bit read width, constructed by IP core generator.

The data in FIFO are sent to the PC by Universal Asyn-chronous Receiver Transmitter (UART). Even though there are various ways for communication [13], UART module can simplify the circuits.

4. SOFTWARE DESIGN

According to PicoBlaze instruction system, control codes

are written in Notepad++, and stored as a PSM format file. And the PSM file is compiled by KCPSM3 compilers, generating a VHDL file storage user programs. Then the VHDL file and PicoBlaze microprocessor soft core are loaded to ISE project, and configure each input and output ports. System software control flow chart is shown in **Figure 5**.

The working process is: the PC sends start instructions to PicoBlaze microprocessor; the microprocessor initializes system settings, and begins to choose excitation electrodes, measuring electrodes; after measuring the first data, the next pair of measurement electrodes is selected and measured, until 13 measurements are finished. Then choose the next pair of incentive electrodes, the measurements will continue until 16 channels are excited. Datasets are immediately sent to reconstruction computer after processing. The program will repeatedly execute until it receives the stop instruction from the computer.

5. RESULTS AND DISCUSSION

To evaluate the system, we carried out tests on a homogenous tank with water in it. The circular tank has 16 stainless electrodes attached around the boundary, as shown in **Figure 6**. A measured differential voltage is displayed in **Figure 7**, as an example, the wave represents the differential voltage between E3 and E4 when E1 and E2 are injected electrodes.

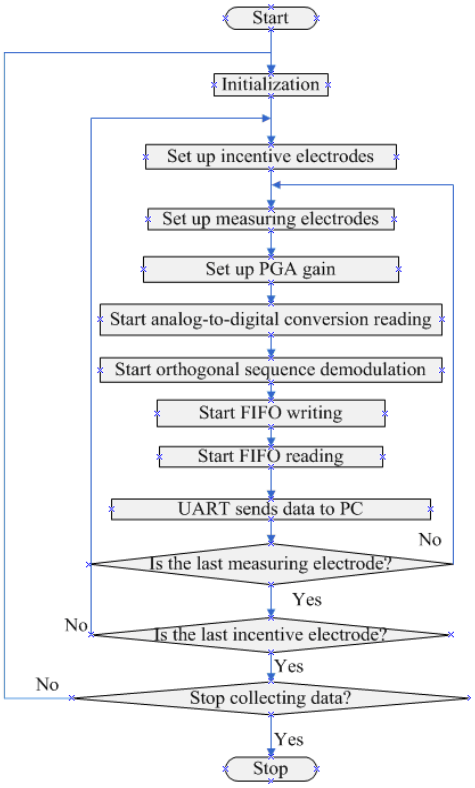

Figure 5. System software control flow chart.

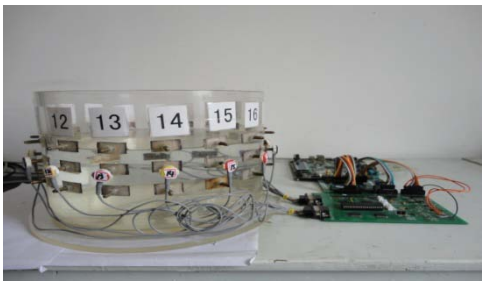

Figure 6. Physical model of the system.

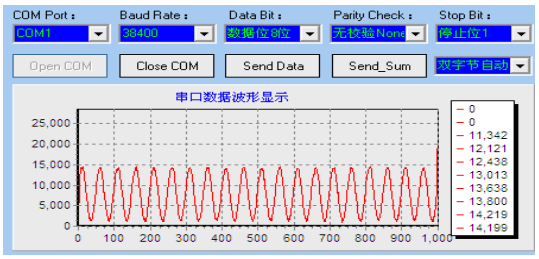

Figure 7. Measured voltage between E3 and E4 when excitation current injects into E1and E2.

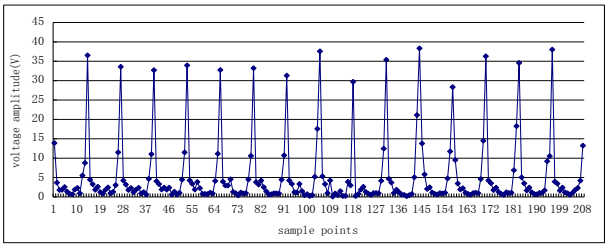

Figure 8. Measured voltage of a homogenous field.

The signal-to-noise ratio (SNR) of the system is calculated according to

$$\mathrm{SNR} = -20\log_{10}\frac{\sigma}{\overline{v}} = -20\log_{10}\frac{\sqrt{\sum_{i=1}^{L}(v_i^2 - \overline{v}^2)}}{\overline{v}} \qquad (8)$$

where, $\overline{v}$ is the average voltages, v_i is the *i*th measured voltage in a measuring period, L is the measuring times.

By 500 times tests, the SNR can achieve 36 dB.

The complex amplitude of a frame including 208 measured voltages is plotted as **Figure 8**.

From the figure, we know that the channels' consistency is not as good as expected. There are several factors affecting the consistency, such as electrodes size, installation spacing, communication cables' impedance, multiplexer circuits and the layout of the board, etc [14-16]. Therefore, we will put more efforts to improve the system from the above aspects.

6. CONCLUSION

It can be seen from the experimental results, 16 elec-

trodes EIT digital data acquisition system can complete the multi-channel voltage signal acquisition and processing. Although there are still some defects left to be further studied and solved. We hope it can take the advantages of digital system to put forward the application of electrical impedance tomography.

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