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Modeling of IEEE1588 on OPNET and Analysis of Asymmetric Synchronizing Error in Smart Substation

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ABSTRACT

The IEEE1588 network time synchronization, matched with smart substation information network transmission, is becoming the next generation advanced data synchronization of the smart substation. It is known that the inherent asymmetry error of the network synchronization approach in the smart substation is highlighted, which is concerned particularly. This paper models the synchronization process of the IEEE1588 based on the communication simulation software of OPNET Modeler. Firstly, it builds the models of master-slave clock, IEEE1588 protocol and network synchronization model, and analyzes the composition and influencing factors of the asymmetry error. Secondly, it quantitatively analyzes the influence of the synchronous asymmetric error of the IEEE1588 affected by the network status differences and the clock synchronization signal transmission path differences. Then its correction method is analyzed, in order to improve the IEEE1588 synchronization reliability and gives the solutions to its application in smart substation.

Keywords: Smart Substation; IEEE1588; Synchronization; Asymmetric Error

1. Introduction

As the important node of the smart grid, the smart substation based on network communication provides grid application oriented integration data platform, its biggest feature and advantage is information sharing [1-3]. The synchronization of high precision data is the important premise and basic properties to realize information sharing. Application system such as relay protection, SCADA, PMU and so on has a high requirement on the data synchronization which is paid much attention as the core problem of smart substation technology [4-6].

At present, the smart substation data synchronization usually adopts IRIG-B, and uses point-to-point link with exclusive fiber optic, sending the unidirectional synchronization signal. This type of flow reliability conflicts with the network information transmission mode of smart substation [7-8]. IEEE1588 as precision clock synchronization protocol matches with Intelligent substation network transmission mode based on IEC61850 [9], can share network resources with other packet, and eliminates the timestamp mark error of NTP/SNTP protocol mode and its synchronization is accurate to sub-microsecond, which is becoming the next generation synchronization mode of the smart substation, with good development prospects.

At the same time, with the inherent defect of uncertain network synchronization, synchronized asymmetry error may occur in the synchronization of IEEE1588 because of differences running state and transmission path in the network.

Under the high data synchronization requirements of smart substation, the issue becomes more prominent [10-12]. At present, due to the lack of quantitative analy-sis tools and methods, the study of IEEE1588 is limited to the field test, the study on the forming mechanism, influence degree and countermeasure of the dissymmetric error is nearly in a gap, which limits its popularization and application [13-14].

This paper develops a IEEE1588 synchronization process modeling of smart substation with a communication simulation software named OPNET Modeler, and analyses the differences of network status and the master-slave clock synchronization signal transmission path quantitatively [15], then studies the influence on IEEE1588 synchronous asymmetry error[16], as also as its correcting method.

2. Asymmetric Synchronizing Error

IEEE1588 precision clock synchronization protocol was promulgated by the IEEE standard committee in 2002, which is to meet the high-precision requirement of the measurement and control applications in a distributed

network of timing synchronization. It's a brand-new attempt to introduce IEEE1588 into power domain that is consistent with smart substation network transmission, and is beneficial to take advantage of information sharing. But as a network synchronization mode, the problem of uncertainty is also prominent which needs to be studied in depth.

2.1. IEEE 1588 Protocol and Synchronization Process

1) IEEE 1588 protocol feature

IEEE1588 protocol is a distributed network synchronization protocol, and it doesn't need networking singly [17]. It can share hardware resources on network, and chooses multiple transmission paths flexibly, also can get the real-time status of other nodes on network. It ensures the reliability of the synchronization system.

Traditional network synchronization time stamp was performed by the software, and the position of time stamp is on application layer, so the message parsing and packaging processing delay constitute a part of synchronization error. As IEEE1588 Protocol time stamps on physical layer exit by hardware using the technology of accessing MAC by Ethernet media, which eliminates part error of time delay, as shown in **Figure 1**.

2) Synchronization process

IEEE1588 synchronization process is shown in **Figure 2**.

Figure 1. Time stamp of network synchronization.

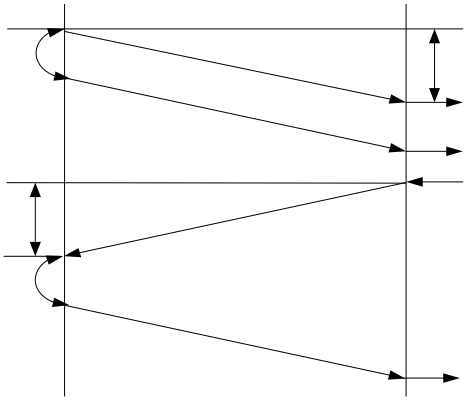

Figure 2. Synchronization process of IEEE1588.

Assuming that the master clock and the slave clock deviation is *offset*, that is $offset = t_{slave} - t_{master}$, the slave clock at the local time t_1 sends synchronization request packets to the master clock, the master clock receives synchronization request packets at the local time t_2. Assuming transmission delay from the slave clock to the master clock is δ_1, so

$$t_2 = t_1 + offset + \delta_1 \tag{1}$$

The master clock sends synchronization packets to the slave clock at t_3, and the synchronization packet includes two time scales as t_2 and t_3. The slave clock receives the synchronization packet at t_4. If transmission delay from the master clock to the slave clock is δ_2, so

$$t_4 = t_3 - offset + \delta_2 \tag{2}$$

All t_1, t_2, t_3 and t_4 are known quantities in formula (1) and (2), but *offset*, δ_1 and δ_2 are unknown quantities. Assumes $\delta_1 = \delta_2$, so the slave clock can solve and correct the time error offset based on the formula (1), so

$$offset = \frac{(t_2 - t_1) - (t_4 - t_3)}{2} \tag{3}$$

2.2. The Influences of IEEE1588 Asymmetric Error

The importance assumption of IEEE1588 synchronization is round-trip transmission path symmetry, transmission delay $\delta_1 = \delta_2$, since the differences in both network status and transmission path dynamics, transmission delay δ_1 and δ_2 generally are not equal, which cannot be deleted directly, so formula (3) should be corrected as:

$$offset = \frac{(t_2 - t_1) - (t_4 - t_3) + \delta_2 - \delta_1}{2} \tag{4}$$

$$\Delta t = \frac{\delta_2 - \delta_1}{2} \tag{5}$$

Δt is asymmetric error, the influences of IEEE1588 asymmetric error mainly includes:

1) The difference of transmission path

Transmission delay δ is composed of link transmission delay D_{link} and switch transmission delay D_{switch}, so

$$\delta = D_{link} + D_{switch} \tag{6}$$

Synchronous packet is stored and forwarded by the switch address analytical table dynamically, as round-trip transmission path may be different when the synchronous packet passes switch and link, D_{link} and D_{switch} are not symmetrical generally. The transfer rate of optical fiber link is 2/3 of velocity of light, that is to say the transmission delay of one 1000-meter link is 5μs. A switch packet processing delay is microsecond level, but

the synchronous precision requirement of IEEE1588 protocol is sub-microsecond level, so the unequal Δt from transmission path cannot be ignored.

2) The difference of network status

The communication running state is dynamic, and running state S_i is closely related to load conditions of network, so the switch processing delay D_{switch} is different under different running state S_i. As a result, even round-trip transmission path is symmetry, as the network status is different, then transmissio n delay δ_1 and δ_2 are not equal.

All the people hold the same attitude that the asymmetric error makes IEEE1588 synchronization precision jitter, but the study of asymmetric error stays on qualitative analysis level because of limited to the research methods. Once the synchronous system of smart substation out of step, the protection device may lock, wrong operator miss operate, even more severe is that the secondary system becomes breakdown. So it is necessary to build a synchronous process simulation model of IEEE1588 and quantitative analysis IEEE1588 asymmetric error and then formulate countermeasures.

3. Synchronous Process Modeling and Asymmetric Error Analysis

IEEE1588 synchronous process model includes master-slave clock model and synchronous network model, and the model reflects several features: IEEE1588 protocol packet processing mechanism, the technique of time stamp on the physical layer exit by hardware, synchronization network made by switch and optical fiber and asymmetric error [18].

3.1. IEEE Master-Slave Clock Model

Figure 3 is based on IEEE1588 master-slave clock model, it mainly completes following several functions:

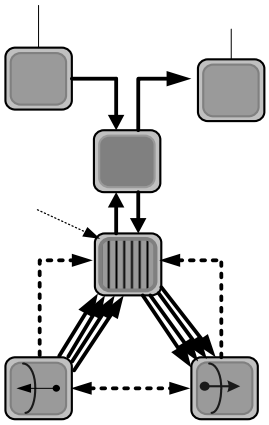

Figure 3. Clock model based on IEEE1588.

1) Synchronous packet formation

Master-slave clock sending model produces four main synchronous packets according to different trigger conditions, master clock produces a Sync packet per second, then put Sync packet sending time T1 on Follow up, after receiving the request Delay_req from slave clock, put receiving time T4 on response Delay_resp packet.

2) IEEE1588 protocol package and analysis

The four main synchronization packets of IEEE1588 are sync, follow up, delay_req and delay_resp, and they have the same format and the same 64Byte long frame with padding bytes, but their time stamps have different information. Use the following up packet model as an example, origin Timestampas master clock sends time T1, and sync interval is synchronous period(usual is 1 second), grandmaster Clock Variance is the change rate of master clock. The data link layer package and analysis packet MAC address, and interface module is general module, completing the protocol analysis and the data packet filling from the data link layer to application layerin IEEE1588.

3) Time stamp marker and read

Different from NTP/SNTP traditional synchronization protocol which is marking and reading time stamp on application layer, time node model of IEEE1588 puts time stamp marker function op_pk_stamp(pkptr) and reading function op_pk_stamp_time_getpkptr) on the exit of the data link layer, to realize time stamp marker and read function of clock, and reduce protocol analysis time.

4) Calculation and correction of Master-slave clock offset and asymmetric error

The slave clock uses formula (7) to calculate and correct master-slave clock offset and asymmetric error Δt.

$$offset_{(i+1)} = offset_{(i)} - T_{(i)} - delay\_offset_{(i)} \quad (7)$$

T is master-slave clock's correction value through the calculation of t_1, t_2, t_3 and t_4 according to formula (3), and *delay_offset* is asymmetric error Δt.

Some codes of master clock model areas follows:

```
/* Setpacket formal,send information and so on,and put sending time t1 on the */
 /* packge of follow_up */
pkptr =op_pk_create (pksize);
t1=(op_pk_creation_time_get(pkptr))*10000000000;
pkptr_Sync=op_pk_create_fmt("Sync");
pkptr_Follow_up=op_pk_create_fmt("Follow_up");
op_pk_nfd_set(pkptr_Follow_up,"originTimestamp",t1);
….
op_pk_fd_set(pkptr,1,OPC_FIELD_TYPE_INTEGER,1,16);
op_pk_fd_set(pkptr,2,OPC_FIELD_TYPE_PACKET,pkptr_Sync,464);
/* Put receiving time t4 of Delay_req packet on
```


response packet*Delay_resp*. */
pkptr = op_pk_get (op_intrpt_strm ());
op_pk_stamp(pkptr);
t4=(op_pk_stamp_time_get(pkptr))*10000000000;
op_pk_nfd_set(pkptr_Delay_resp,"originTimestamp",t4);
Some codes of slave clock model areas follows:
/* Calculate and correct master-slave clock *offset* and asymmetric error*delay_offset*. */
T=((*t2-t1*)-(*t4-t3*))*0.5;
delay_offset=((t2-t1)+(t4-t3)) *0.5;
offset=offset-T- delay_offset;

3.2. Network Synchronization Model

Network synchronization model includes running status network model, transmission path network model, the switch with 500000 p/s processing capacity and the100M optical fiber link, shown as **Figure 4**. In **Figure 4(a)**, to observe the transmission delay with different network running status, inject background traffic into switch. In **Figure 4(b)**, to observe the transmission delay with different transmission path, increasing the number of switch from 0 to 3 on master-slave synchronous packet transmission path.

Different network running status

3.3. Asymmetric Error Simulation

Table 1 is the performance of transmission delay, injects different background traffic to the switch. When background traffic is 25%, transmission delay is 262.993 μs, which costs 1 μs more compared to transmission delay without background traffic. Transmission delay becomes 2.667 μs when background traffic is 40%. When background traffic increases to 95%, transmission delay is 337.993 μs. Value of transmission delay varies from 0.211 μs to 76 μs on different background traffic, and it enlarges constant. Asymmetric error Δt fromdifferent network running status couldnot be ignored.

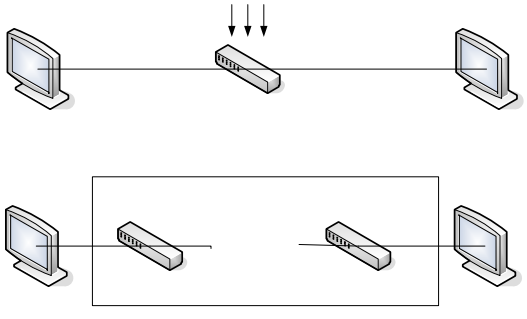

Figure 4. Network synchronization model.

2) Different transmission path

From **Table 2**, when the number of switch increases one more, transmission delay will increase 87. So when configuration of communication network switch change and master-slave clock round-trip transmission path differ one or one more switch, correction of asymmetric error Δt must exist.

So assumption of master-slave clock round-trip transmission path is equal exists defect, asymmetric error from different network status and transmission path should be a necessary link of synchronous correction.

4. Asymmetric Error Correction

There are some differences between smart substation communication network and general LAN: 1) the structure of network is simple. Configuration of smart substation secondary system is normative according to voltage level, the number of devices are limited, switches are no more than four in general; 2) Traffic flow is specific. All automatic business such as measurement, protection, test and control and etc. have their corresponding *SV/GOOSE/MMS*/Synchronization information flow, and the feature of information flow is specific, little uncertain flow. Specific feature of smart substation communication network makes asymmetric error correction feasible.

4.1. Asymmetric Error Correction Method

Assuming at time t, master-slave clock transmission delay is measured by network monitoring device.

Table 1. Impact of background traffic on transmission delay.

Background traffic	Delay(μs)
0%	261.993
5%	262.204
10%	262.438
20%	262.993
40%	264.660
80%	277.993
95%	337.993

Table 2. Impact of path on transmission delay.

The number of switch	Delay(μs)	The increase of transmission delay(μs)
0	88.553	/
1	176.207	87.654
2	261.993	85.786
3	349.145	87.152

$$\delta_{1t} = D_{link1t} + D_{switch1t} \quad (8)$$

$$\delta_{2t} = D_{link2t} + D_{switch2t} \quad (9)$$

According to formula (5), asymmetric error Δt_t is:

$$t_t = \frac{\delta_{2t} - \delta_{1t}}{2} \quad (10)$$

Put Δt_t from formula (10) into master-slave clock correction, that is $delay\_offset(i)$ in formula (7).

Since δ_{1t} and δ_{2t} are got from measurement in operation, correction error exists because of measurement.

4.2. Asymmetric Error Correction Simulation Analysis

1) Simulation scenario setting

Asymmetric error correction simulation model is shown as **Figure 5**. Master clock transmission path is from *switchA* to slave clock, while return path is composed of EDCB.

Setting parameters of asymmetric error simulation as **Table 3**:

2) Analysis of asymmetric error simulation results

Results of asymmetric error simulation are shown in **Figure 6**. Curve1 is uncorrected asymmetric error Δt, from 0 to 34 s, range of Δt is 0-0.987 μs, synchronous error less than 1 μs, from 35s to 100s, with the increasing background traffic, Δt enlarges to 1.143-41.937 μs. Obviously Δt has completely over the minimum requirement that IEEE1588 synchronous precision should less than 1 μs. At the time of 101s, 116s and 131s, the number of slave clock path switch turn into 2, 3 and 4, Δt enlarges to 43.5010-136.169 μs further.

As correction error is 1%, *curve2* is asymmetric error Δt which uses the corrected method of this paper to correct. From 0 to 100s, and when master-slave round-trip switches have the same number, the range of background traffic is 0-100%, Δt is 0-0.419 μs after correction. From 101 to 130s, the differ number of round-trip switch is 2, and the range of background traffic is 0-14%, Δt increases to 0.435-0.909 μs. At the time of 131s, the number of switch turn into 3, Δt is1.305 μs, over 1 μs, and it cannot meet the requirement of IEEE1588 synchronous precision.

Curve3 is the change condition of Δt after correction when assume correction error is 0.5%. The range of Δt is 0-0.681 μs after correction, even the differ number of master-slave round-trip is 3, it still can meet the precision requirement of 1 μs.

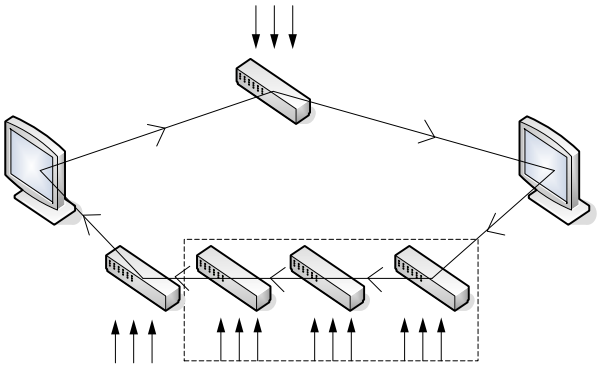

Figure 5. Synchronization network model in asymmetric error simulation.

Table 3. Parameters of asymmetric error simulation.

Simulation time(s)	Path of master-slave clock		Path of slave-master clock	
	switch	Background traffic(%)	switch	Background traffic(%)
0-100	A	0	B	0-100
101-115			CB	
116-130			DCB	0-14
131-145			EDCB	

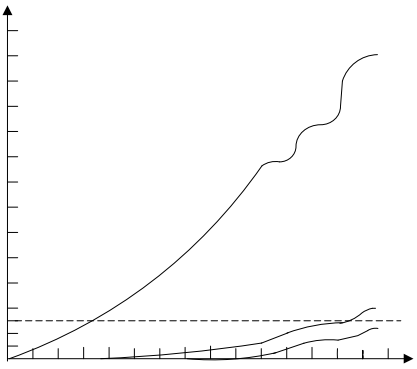

Figure 6. Results of asymmetric error simulation

To sum up, asymmetric error Δt of master-slave clock link impacts IEEE1588synchronous precision seriously, while the correction method of this paper will reduce the impact of asymmetric error greatly. Relative certainty of smart substation communication network makes the measurement of δ_{1t} and δ_{2t} feasible, the problem of asymmetric error of network synchronization can be solved effectively by the error correction which is according to this.

5. Conclusions

This paper develops IEEE1588 synchronous process model, quantitatively analyses asymmetric error from network running status and the difference of master-slave clock transmission path, researches that the correction can supply a new approach and method expecting for actual

measurement for the quantitative analysis ofIEEE1588 synchronization process, and develops research thought of IEEE1588 synchronization uncertainly problem.

Although IEEE1588 has necessitated solved questions, IEEE1588 adapts to the development trend of smart substation network transmission. To search and improve reliable method of IEEE 1588 synchronization, overcome network uncertainly shortcomings, make full use of network synchronization is the inevitable trend for the synchronization technique of smart substation.

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