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Fast CR-SRAM Using New Charge-Recycling Scheme

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ABSTRACT

In this paper, a CR-SRAM using new charge recycling scheme is described, novel bit-line pre-charge voltage distribution is proposed. The SRAM pre-charge voltage level is designed by logarithm instead of linear. The new design leads to improvement in speed compared to the original CR-SRAM. Simulation results show that the new CR-SRAM using novel pre-charge voltage distribution scheme reduced the write access time by 34% with 9% power dissipation penalty.

Keywords: SRAM; Lower-Power; Charge-Recycling

1. Introduction

As the demands for handheld devices and other battery-supplied equipments increase, more and more attention has been paid on low power IC design. SRAM takes a large power dissipation of the whole chip. Many low power SRAMs has been designed [1]. One important way to reduce SRAM power dissipation is reducing the power consumed by bit-line. During write and read operation, the bit-line voltage swing is full, charging and discharging of the highly capacitive bit-lines consumes a lot of energy.

Reducing the bit-line power consumption during write cycle is an effective way to reduce the power dissipation. Recently, a low power using bit-line charge-recycling technology has been reported [2]. The charge recycling concept was firstly introduced in the low power on-chip bus architecture design [3], B. D. Young apply this technology to ROM [4]. Kim applied charge-recycling directly to the bit-line to reduce dynamic write power associated with bit-line swing in SRAM [1]. The main idea of this technique is that the charge stored in the bit-line during one write cycle can be recycled for the next write operation, which leads to reduction of power dissipation to $1/N^2$, while N is the bit-line pair number.

However, the original CR-SRAM has two disadvantages. Firstly, the access time of write operation is long, the operation frequency is limited. Secondly, when the recycle time increase, the voltage interval began to getting small, which lead to SNM decrease when the recycling time rise.

In this paper, a new charge-recycling scheme is proposed to further enhance the performance and stability of CR-SRAM. The logarithmic pre-charge voltage is applied to write operation. To verify the new charge recycling scheme, a prototype 2 Kbits Charge-Recycling SRAM is implemented and simulated in SMIC 0.13 μm CMOS technology. The simulate results exhibit the write speed is 34% faster than original design. The average power dissipation per write cycle is 2.4 μW at 1.5 V supply.

The rest of the paper is organized as follows: In section II, the new charge recycling scheme is introduced. In section III, a prototype 2 Kbits SRAM using the new charge-recycling scheme is built and simulated, the performance of new CR-SRAM is also analyzed.

2. New Charing Recycling Scheme

The proposed new charge recycling scheme is that the pre-charge voltage distribution is logarithmic instead of linear. The pre-charge voltage is given by the following function.

$$y = \frac{\ln(1+\mu x)}{\ln(1+\mu)} \quad 0 \le x \le 1 \tag{1}$$

Equation (1) is used in Pulse Code Modulation as an unequal quantization method in the area of communication. The μ is called compression factor. The μ law function is illustrated in **Figure 1**. When $\mu = 0$, the function is linear. When μ increase, the curves are more apart from linear. The function is odd symmetry.

The new pre-charge voltage is calculated as follow. Firstly, determine the compression factor μ and charge-recycling bit-line pair number *N*. Secondly, divide the supply voltage range into tow parts, 0 to $V_{DD}/2$ and $V_{DD}/2$ to V_{DD}. In the $V_{DD}/2$ to V_{DD} range, replace y axes range with $V_{DD}/2$ to V_{DD}, calculated the voltage value by

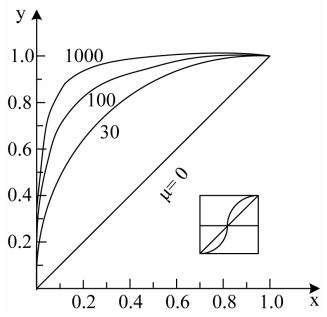

Figure 1. μ law bit-line voltage.

x equal 1/2 and 3/4, In the range 0 to $V_{DD}/2$, the voltage value is calculated similarly. When the charge-recycling bit-line pair number N is 4, and μ = 1, the pre-charge voltages is 1.41 V, 1.19 V, 0.40 V, 0.17 V.

When the pre-charge voltages is determined, mapping each voltage level to SRAM circuit through corresponding resistors. In the proposed SRAM illustrated in **Figure 2**, the corresponding resistors are R1 to R5.

This CR-SRAM using new pre-charge scheme has two advantages compared to the original CR-SRAM, the write speed is improved and the static noise margin is increased.

2.1. Imporve the Write Speed

The write speed is limited by the time which taken by the maximum voltage of bit-line increased to V_{DD}. As is showing in **Figure 3**, the maximum voltage level is V1, which is 1.31 V. The bit-line is charged by supply V_{DD}, the voltage change is slow compared to other bit-line pairs. The circumstance is same as V4, which is discharged by source-line V_{SS}. V1 and V4 take the longest time since that the bit-line is connected to source-line while the other bit-line pair are charge and discharged by the parasitical capacitors. When the bit-line voltage level is designed according to (1), the time consumed by the V1 charged to V_{DD} is short since the voltage is higher than the original V1, which is same as V4, the voltage is lower than original. The logarithmic voltage design makes the time consumed by the bit-line pairs in evaluate phase more equally, and consequently lead to write speed improvement.

2.2. Increase SRAM Static Noise Margin

Another advantage is the SNM is not decreased crucially when the charge recycling time increase. The original bit-line pre-charge voltage level is given by (2).

$$\left[\left(2\cdot N-2\cdot i+1\right)/2\cdot N\right]\times V_{DD}\quad i=1,2,\cdots,N \qquad (2)$$

For N = 4, according to (2), the pre-charge voltage are 0.19 V, 0.56 V, 0.91 V, 1.31 V. The bit-line voltage is decreased due to the charge leakage in write cycle. Every time the charge recycled for one write operation, the voltage decreased after the bit-line pair connected to evaluate, which lead to the voltage margin in the last few

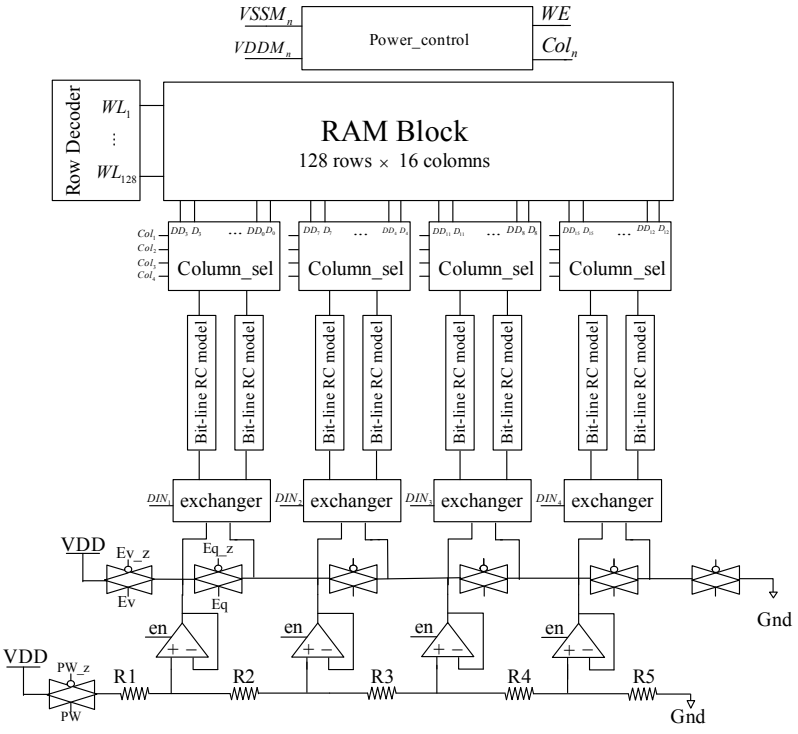

Figure 2. CR-SRAM architecture using new pre-charge voltage distribution scheme.

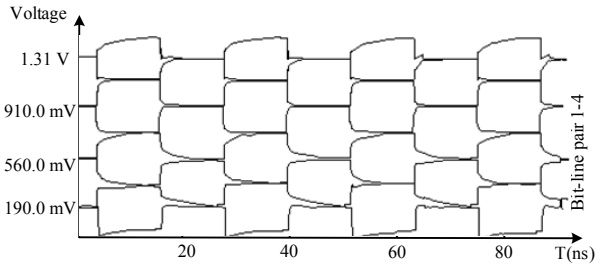

Figure 3. Simulated waveform of original CR-SRAM.

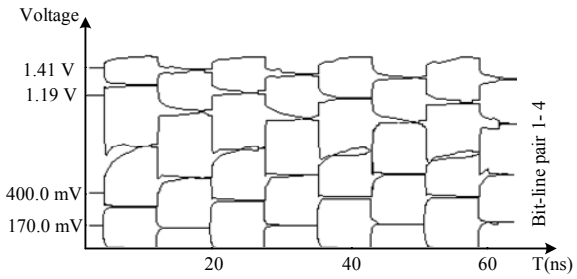

Figure 4. Simulated waveform of proposed CR-SRAM.

write cycle getting small. The SNM of SRAM is limited by the smallest voltage difference of the last write cycle.

3. SRAM Simulation and Results

To demonstrate the concept of the proposed charge- recycling scheme, a 2 K bits CR-SRAM has been designed and simulated in SMIC 0.13 μm CMOS technology. As is showing in **Figure 2**, the main blocks are illustrated below.

- The exchanger block is used by bit-line pair for charge-recycling. If the number of exchangers is N, the charge will recycled for N times.
- The Bit-line RC model block is a π RC model of electronic wire. The values of capacitors and resistors are determined by the technology file provided by the Fab.
- To make data write in SRAM cells correctly, the power control block is dedicated to floating the source line during write operation. The source line VDD and VSS are disconnected from the RAM Cell to ensure data write in with limited bit-line voltage [5]. During SRAM data retention period, VSS is connected to positive bias voltage to reduce power dissipation.
- The pre-charge circuit is implemented by a unit gain buffer which has rail-to-rail swing. To enhance output voltage swing, complementary PMOS and NMOS difference amplifier is used.

During simulation, the control signals are provided to generate four consecutive write operations, which consist a charge-recycling cycle. The simulated waveforms of original and proposed CR-SRAM are show in **Figures 3** and **4**.

From the simulated waveforms of proposed CR-SRAM and original CR-SRAM, the write speed of new CR-SRAM is improved 34% compared to the original one. Meanwhile, the power dissipation of new CR-SRAM is 2.4 μW, and the original CR-SRAM consumes 2.2 μW per write access, the power dissipation is increased about 9%. Besides, the original CR-SRAM bit-line voltage margin shrink due to charge leakage, the bit-line voltage margin of proposed CR-SRAM is enhanced.

4. Conclusion

Recycling the charge of bit-line for multiple write operation is an effective way to decrease SRAM power dissipation. CR- SRAM can reduce the power dissipation to $1/N^2$. The logarithmic pre-charge voltage is proposed to further optimize write speed. According to simulated results, the write speed is improved by 34%, while the power dissipation increased 9%.

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