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Discharge Characteristics of a Triple-Well Diode-String ESD Clamp

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Abstract

In this work, DC and transient characteristics of a 4 diode string utilizing triple-well technologies as a V_{DD}-V_{SS} clamp device for ESD protection are analyzed in detail based on 2-dimensional device and mixed-mode simulations. It is shown that there exists parasitic pnp bipolar transistor action in this device leading to a sudden increase in DC substrate leakage if anode bias is getting high. Through transient simulations for a 2000 V PS-mode HBM ESD discharge event, it is shown that the dominant discharge path is the one formed by a parasitic pnpn thyristor and a parasitic npn bipolar transistor in series. Percentage ratios of the various current components regarding the anode current at its current peaking are provided. The mechanisms involved in ESD discharge inside the diode-string clamp utilizing triple-well technologies are explained in detail, which has never been done anywhere in the literature based on simulations or measurements.

Keywords

ESD Protection, Diode String, Triple Well, Device Simulation, CMOS, RF IC

1. Introduction

CMOS chips are vulnerable to electrostatic discharge (ESD) due to thin gate oxides used, and therefore protection devices are required at input pads. Larger size is preferable for the protection devices to reduce discharge current density and thereby to protect them against thermal-related problems. However, adopting large size tends to increase parasitic capacitances added to the input nodes generating other problems such as gain reduction and poor noise characteristics in RF ICs [1].

To reduce the added parasitics, various techniques have been suggested. However, basic approaches should be to reduce size of protection devices con-

nected to input nodes, and protection schemes utilizing diodes are most popular in RF ICs [2] [3] [4].

In a diode input protection scheme, it is needed to include a V_{DD}-V_{SS} clamp device such as an NMOS transistor in the input pad structure to provide discharge paths for all possible human-body model (HBM) test modes.

In a diode input protection scheme utilizing an NMOS clamp device, critical peak voltages developed across gate oxides of an input buffer in an ESD event are determined by the sum of the forward voltage drop across the diode device and the V_{DD}-V_{SS} clamping voltage, which is equal to the snapback voltage of the NMOS clamp device [5]. Hence, as gate oxides are getting thinner, the snapback voltage, which cannot be engineered much, becomes an obstacle in using the NMOS clamp device further. Besides, the snapback voltage of the NMOS clamp device determines the amount of critical lattice heating inside the ESD diode device connected between the input node and the V_{DD} bus [6]. Hence it is clear that we have to find some way to reduce the V_{DD}-V_{SS} clamping voltage.

A diode string connected in a forward conduction mode was suggested as a V_{DD}-V_{SS} clamp device for low voltage technologies [7]. Diode strings can reduce the V_{DD}-V_{SS} clamping voltage since the number of diodes in series connection will determine the forward turn-on voltage during an ESD event. Since there is no snapback behavior in these devices which appears in NMOS devices, there is no danger of inducing large voltages on gate oxides of input buffers for long time [5].

While it was expected that increasing the number of diodes in series can control the leakage current for a given supply voltage by increasing the turn-on voltage of a diode string, it turned out that a leakage mechanism involving parasitic pnp bipolar transistor action puts a limitation in using the device at a higher supply voltage [7]. Furthermore it turned out that pnpn thyristor action inside the diode string becomes another obstacle by generating a DC snapback behavior with a low holding voltage [8].

A diode string design utilizing a triple-well technology was suggested to reduce the leakage by suppressing parasitic pnp bipolar transistor action [9], and they showed by experiments that the substrate leakage current is reduced a lot by adopting triple wells. However the leakage current presented in [9] seems not to include a leakage to the n+ cathode of the diode string, which is also connected to the ground. Therefore it seems they used an improper definition of leakage for this device. In [9], they presented data regarding ESD robustness of the chips equipped with the ESD protection circuit utilizing the triple-well diode-string clamps. However they didn't explain about transient discharge behavior of the clamp device.

In this work, we analyze in detail DC and transient discharge characteristics of a triple-well diode string as a clamp device for ESD protection based on 2-dimensional (2-D) device simulations and mixed-mode transient simulations.

In Section 2, we introduce the diode protection scheme utilizing a triple-well

diode string as the clamp device, and presents a cross section diagram of the device. In Section 3, we explain DC simulation setup and analyze simulation results. In Section 4, we present an equivalent circuit model for a CMOS chip equipped with the protection devices, and provide human-body model (HBM) mixed-mode transient simulation results with detailed analyses to show how the ESD protection scheme utilizing the triple-well diode string clamp can protect CMOS chips. Section 5 concludes the work.

2. Protection Scheme and Device Structure

Figure 1 shows the diode input protection scheme. A 4-diode string is assumed as the V_{DD}-V_{SS} clamp device, which replaces the popular grounded-gate NMOS transistor. In Figure 1, a CMOS inverter is assumed as an input buffer. In Figure 1, the discharge path for a PS mode is shown, which is regarded as the weakest mode among HBM discharge events [5]. A PS mode represents the test mode, where a positive ESD voltage is applied to an input pin with a V_{SS} pin grounded. The forward-biased diode D_2 and the forward-biased diode-string clamp D_3 in series forms a discharge path. Here we assume that D_3 conducts as a forward-biased 4 diodes in series, which will be shown quite not true.

In Figure 2, a cross section diagram of a triple-well 4-diode string is presented, where a parasitic pnp bipolar transistor relating each n well is described, which supposedly never turns on since the emitter and the base terminals are shorted as shown. R_{sub} at the right-hand side describes a distributed substrate resistance. For the device used for simulations in this work, anode contact spacing in each diode is assumed as 2.4 μm and the resulting device length in x direction is 37.2 μm. The deep n-well depth and the p-well depth are assumed as about 1.6 μm and 0.7 μm, respectively, and the device depth in y direction is set as 5 μm.

In Figure 2, the 4 series diodes are named as Ds1, Ds2, Ds3, and Ds4 to facilitate explanations regarding conduction mechanisms hereafter. Also the relating p wells and deep n wells are named as pw1~4, and Dnw1~4, respectively. We will call the n^+ diffusion inside Dnw1 by Da1 (which denotes deep n-well anode of Ds1), and the p^+ and the n^+ diffusions inside pw1 by Pa1 (which denotes

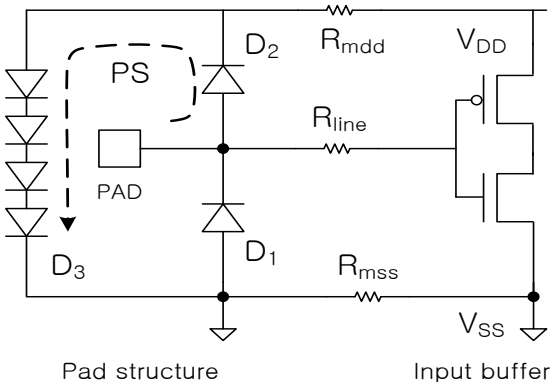

Figure 1. Diode input protection scheme using a 4-diode string clamp device.

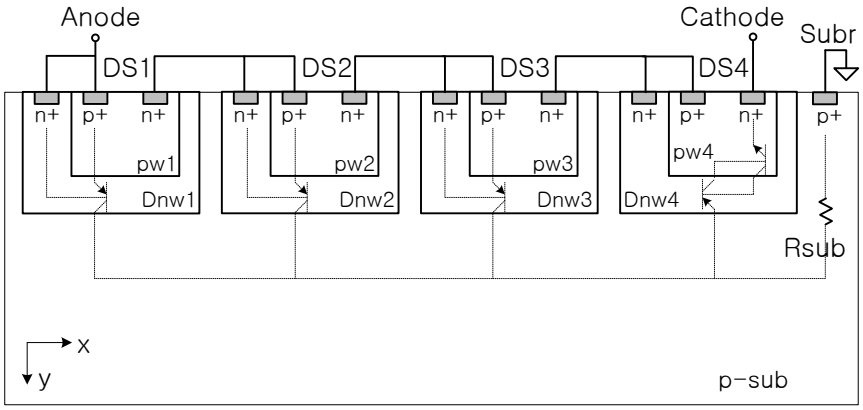

Figure 2. Cross section diagram of a triple-well 4-diode string.

p-type anode of Ds1) and Nc1 (which denotes n-type cathode of Ds1), respectively. Subsequent diffusions will be called in a similar fashion. Therefore diffusions inside Ds4 will be called by Da4, Pa4, and Nc4.

As shown in Figure 1, the Anode and the Cathode contacts of the device shown in Figure 2 are connected to a V_{DD} bus and a V_{SS} bus, respectively. As shown in Figure 2, the Subr contact, which denotes a substrate contact at the right-hand side corner, is also connected to a V_{SS} bus.

We also denoted an npn/pnp transistor pair around the 4th deep n well in Figure 2 to describe a parasitic pnpn path starting from the p substrate to the Cathode.

3. DC Characteristics

DC simulation was performed on the 4-diode string similar to that shown in Figure 2 utilizing a 2-D device simulator ATLAS [10]. All necessary physical models including an impact ionization model were considered in the simulation. The lattice heating model was deactivated for the DC simulation since lattice heating in a higher current regime tends to be exaggerated when compared to that in a real measurement. The Cathode and the Subr contacts shown in Figure 2 were grounded, and the Anode bias was varied for simulation.

Figure 3 shows simulated currents vs. Anode voltage characteristics of the 4-diode string in a semi-log scale. The Anode, the Cathode (Nc4), and the Subr currents are plotted. The current values are for 1 μm of device width in z direction.

As shown in Figure 3, magnitude of the Anode current is close to that of the Subr current below 0.5 V of the Anode bias. This current must be the sum of leakage currents through the 4 reverse-biased Dnw/psub junctions. Above 0.5 V, magnitude of the Anode current is close to that of the Nc4 current, which must be the current through the 4 diodes in series in the diode string. Notice that this current may be that through the 4 diode-connected npn bipolar transistors in series. We note that by monitoring each component of the Anode current, we could confirm that the Anode current flows dominantly through the Ds1 diode

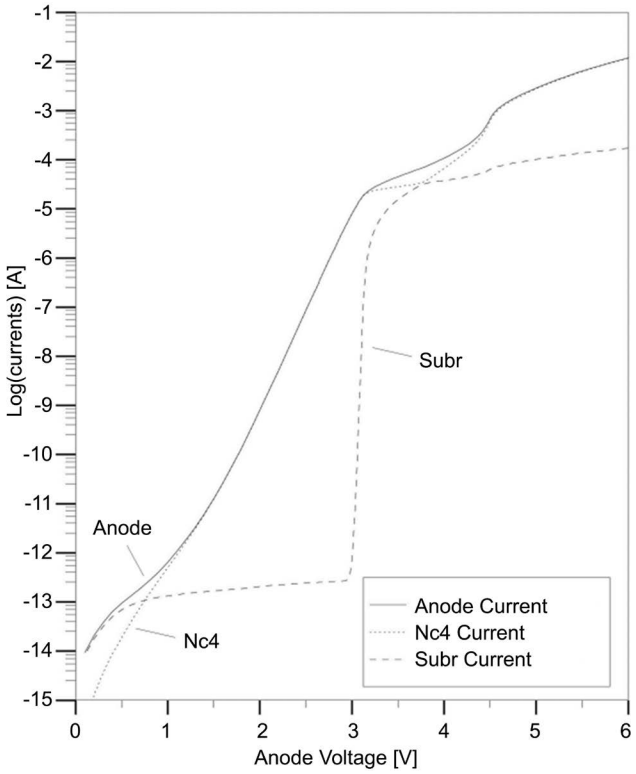

Figure 3. DC currents vs. Anode voltage characteristics of the 4-diode string clamp.

below 1.5 V, and then dominantly through the collector of the Ds1 npn transistor above 1.6 V.

At about 3 V, there is a sudden increase in the Subr current, which is caused by triggering of the parasitic pnp transistor relating the 1st deep n well denoted in **Figure 2** even though the n^+ Da1 and p^+ Pa1 contacts are shorted together. The triggering mechanism can be explained as follow. As the Anode bias is increased, larger portion of the injected electrons from the cathode (Nc1) to the anode (pw1) due to increased forward-biasing of Ds1, diffuses out to reach the bottom-side collector (Dnw1), and flows out to the Da1 terminal. This lowers the potential of the bottom-side Dnw1 region to forward-bias the pw1/Dnw1 junction to trigger the pnp transistor formed by the emitter (pw1), the base (Dnw1), and the collector (p substrate) resulting the abrupt increase in the Subr current. We note that this kind of abrupt increase in the measured substrate current was reported in [9].

At 3.75 V of the Anode bias, the Anode current flows out to the Nc4 and to the Subr terminals in an equal amount as shown in **Figure 3**. Above 3.75 V, the Nc4 current increases fast to become a dominant portion of the Anode current again at 4.5 V. Why the Nc4 current to start to increase fast again? There must be a mechanism to force a sudden increase of current from the Anode to the Cathode (Nc4).

To explain the mechanism involved, we show the internal substrate voltage and the n^+ Da4 voltage, which is the anode voltage of Ds4, in **Figure 4**. We note

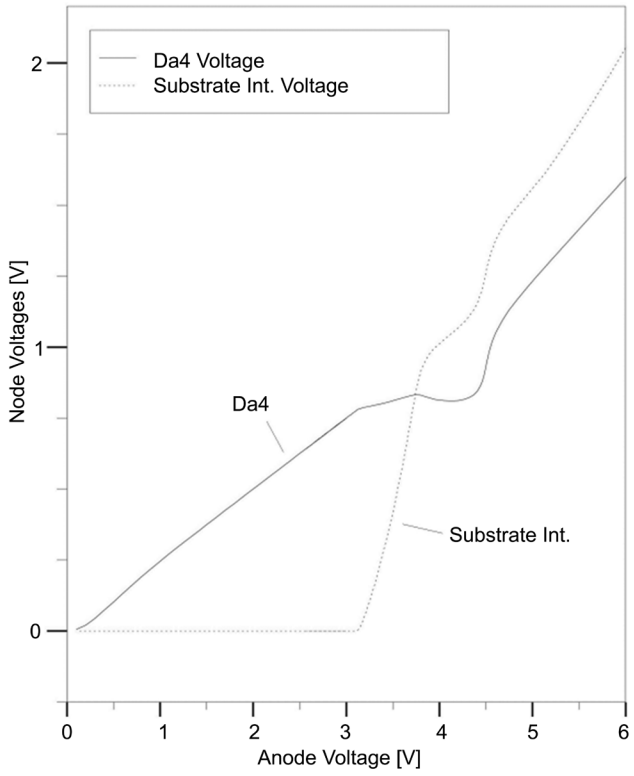

Figure 4. DC internal voltages vs. Anode voltage characteristics.

here that the internal substrate represents the bottom plate of the device shown in **Figure 2**. We note here that these voltages can be probed only in simulations.

As shown in **Figure 4**, the internal substrate voltage increases abruptly at around 3.1 V, which must be a result of the pnp transistor trigger. **Figure 4** also shows that at 3.75 V, the potential of the internal substrate starts to exceed that of the Da4 diffusion, which indicates that the p-substrate/Dnw4 junction can get forward-biased to trigger a pnpn thyristor path formed by Pa1/Dnw1/p-sub/Dnw4. This current must be flowing out to the Nc4 terminal through the npn transistor formed by Dnw4/pw4/Nc4, causing a fast increase in the Nc4 current at 3.75 V in **Figure 3**. Notice that this voltage (3.75 V), which can be regarded as a holding voltage for the series-connected pnpn thyristor and npn transistor, is large enough to avoid its triggering during chip operation with a normal supply voltage.

It is hard to confirm here how hard the 4-series diode-connected transistor path turns on or whether some other pnpn paths inside the device turn on since we cannot probe currents through internal nodes in DC simulations, similarly as in real measurements. However, we will answer for these questions using the transient simulation results in Section 4.

4. Transient Discharge Characteristics

Figure 5 shows an equivalent circuit of an input PS-mode HBM test situation. The portion indicated as "Test environment" in **Figure 5** is an equivalent circuit

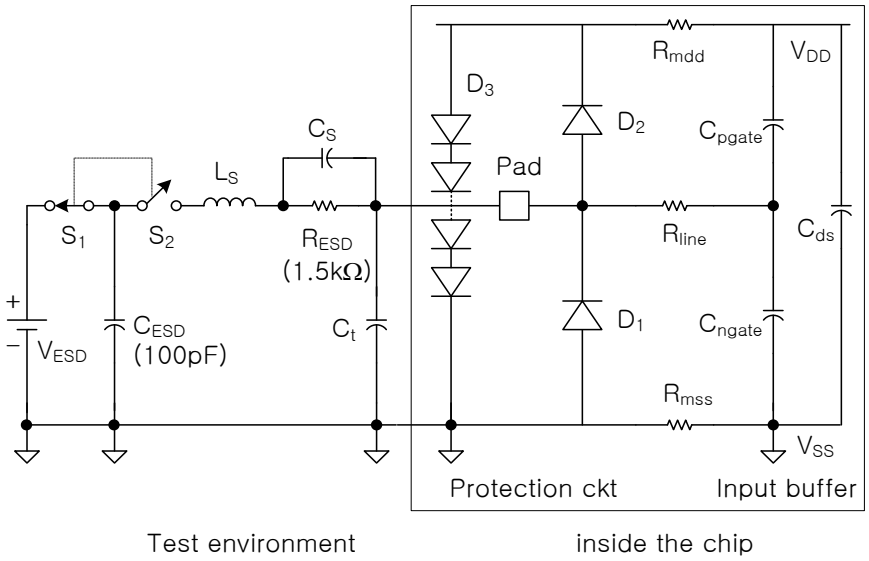

Figure 5. Equivalent circuit of an input PS-mode HBM test situation.

for test equipment connection. C_{ESD} and R_{ESD} represent a human capacitance and a human contact resistance, respectively. Values for other parasitic elements are described in [5]. V_{ESD} is a HBM test voltage, and a switch S1 charges C_{ESD} and then a switch S_2 initiates discharge.

In **Figure 5**, D_1, D_2, and D_3 form a protection circuit at the input pad. A CMOS inverter is assumed as an input buffer inside a chip, which is modeled by a capacitive network. C_{ngate} and C_{pgate} represent gate-oxide capacitances of the NMOS transistor and the PMOS transistor in the CMOS inverter, respectively. C_{ds} represents the n-well/p-substrate junction capacitance.

Utilizing ATLAS, PS-mode mixed-mode transient simulation using the equivalent circuit in **Figure 5** was performed. Differently from the DC simulation in Section 3, a lattice-heating model including joule heat, generation-recombination heat, and Peltier Thomson heat was activated to analyze lattice temperature-related problems also.

The 4-diode string used for the DC simulation was used for D_3 in **Figure 5**. We note that we connected each diode inside the diode string using a 1mΩ resistor to monitor the currents flowing into the two anodes (Da and Pa) of each series diode by monitoring the current through each resistor. Notice that monitoring these internal currents is possible only in simulations, not in measurements.

The reference diode in **Figure 4** of [6] and the 2-cathode diode in **Figure 5** of [6] were used for D_1 and D_2 in **Figure 5**, respectively. The 4-diode string device D_3 replaced a conventional NMOS transistor clamp used in [6]. Therefore we can see any advantage we obtain by adopting this protection scheme utilizing the diode-string clamp.

For PS-mode mixed-mode transient simulation, the V_{SS} node was grounded and V_{ESD} = +2000V was applied. Widths of the protection devices were set as 15

μm, 15 μm, and 200 μm for D_1, D_2, and D_3, respectively as in the case of using the NMOS clamp, where we intended to maintain peak lattice temperature inside all the protection devices below 500˚K [6].

Figure 6 shows variations of discharge currents inside the 4-diode string clamp D_3 in a PS mode as a function of time up to 1μsec after S_2 in Figure 5 is closed. The Pa1, Da1, Pa4, Da4, and Nc4 terminal currents are plotted. The sum of the Pa1 and Da1 currents is also plotted, which corresponds to the Anode current.

The Anode current peaks up to 1.32A within 7.2ns after S_2 is closed, and most of the Anode current flows out to the Cathode (Nc4) terminal, which indicates that the current to the Subr terminal is insignificant. The sum of the Pa4 and Da4 currents corresponds to the current through the series-connected 4 npn transistors, which is supposedly the series diode current originally intended in this device. We can see that magnitude of this current is much less than 50% of that of the Anode current for the main discharge duration. This implies that the rest of the Cathode current must be the current coming into Dnw4 by way of the p-type substrate.

Then, where does this current come from inside the diode string? Certainly one of the starting points of this current must be the Anode terminal. This means that there is at least one pnpn path formed by Pa1/Dnw1/p-sub/Dnw4 in this device. The current through the pnpn path must be flowing in series through

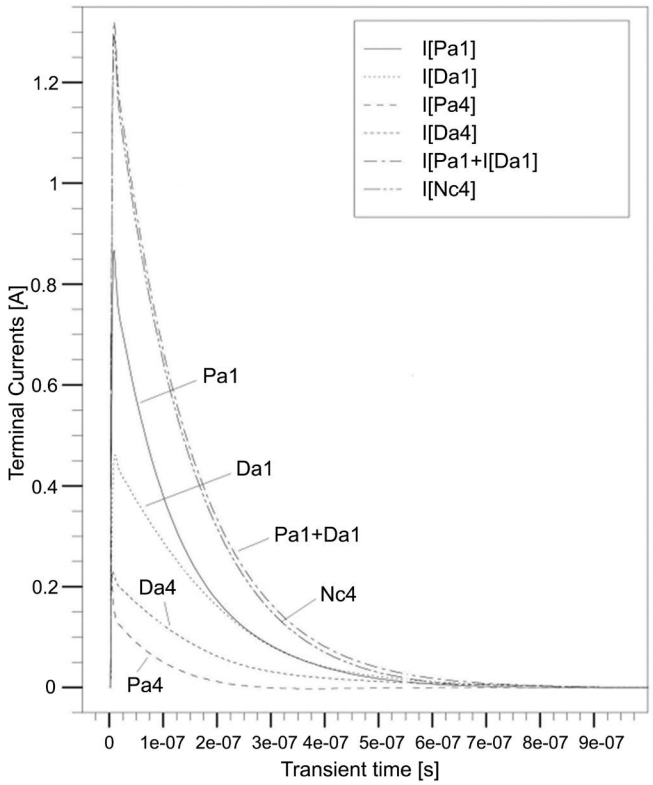

Figure 6. Variations of discharge currents inside the 4-diode string clamp D_3 in a PS mode discharge.

the npn transistor formed inside Dnw4 in Figure 2 as explained regarding the DC simulation results in Section 3.

We note here that triggering of two other pnpn paths reaching Dnw4 is possible, which are the one formed by Pa2/Dnw2/p-sub/Dnw4 and the other formed by Pa3/Dnw3/p-sub/Dnw4. However the potential of Pa1 is highest, and therefore the pnpn path relating Pa1 will turn on first.

By monitoring in detail the variation of Da and Pa currents in each diode in the diode string, we confirmed that all the diodes start to conduct within 0.5ns after S_2 is closed, and the npn collector (Da) currents exceed over the diode (Pa) currents about 3.5ns later.

To make reader to understand the situation easier, percentage ratios of the discharge current components regarding the Anode current in the 4-diode string clamp at its current peak are given in Figure 7. As shown in Figure 7, the current through the series-connected 4 npn transistors, which is assumed as equal to the sum of the Da4 and Pa4 currents, is only 28.4% of the Anode current. 69.5% of the Anode current flows into the Dnw4 by way of the 3 pnpn paths and flows out to the Nc4 terminal. The 3 pnpn paths are those starting from Pa1, Pa2, and Pa3. Only 2.1% of the Anode current flows out to the Subr terminal.

We note that this transient mechanism relating ESD discharge in the diode string clamphas never been explained in detail anywhere in the literature based on simulations or measurements.

From the same simulation result, we showed in Figure 8 variations of the voltages developed on C_{ngate} and C_{pgate} in Figure 5 as a function of time, which correspond to the voltages developed across the gate oxides of the NMOS and PMOS transistors in the input buffer in Figure 1. The pad voltage, which is not shown in Figure 8, is almost same with the voltage developed on C_{ngate}.

In the early stage of discharge, the voltage on C_{ngate} shown in Figure 8 peaks up to 14.9V for a very short duration in the range of a few nanoseconds, which is regarded as not harmful to the gate oxides of the input buffer [5]. This voltage

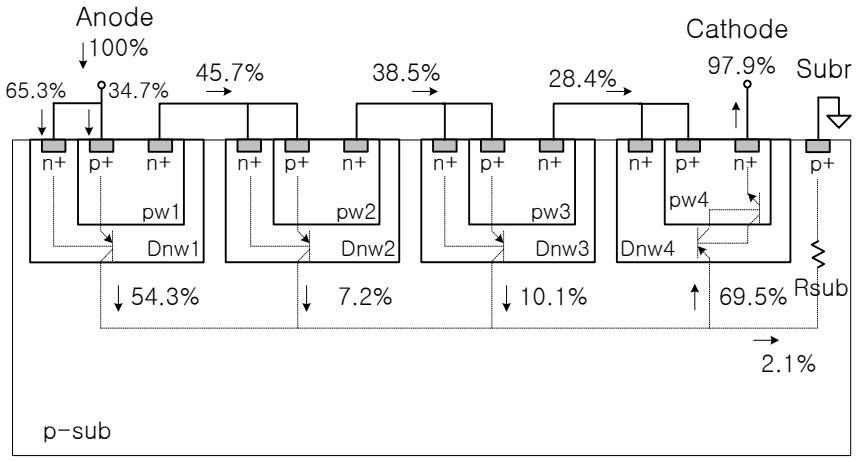

Figure 7. Percentage ratios of the discharge current components in the 4-diode string clamp at its current peak.

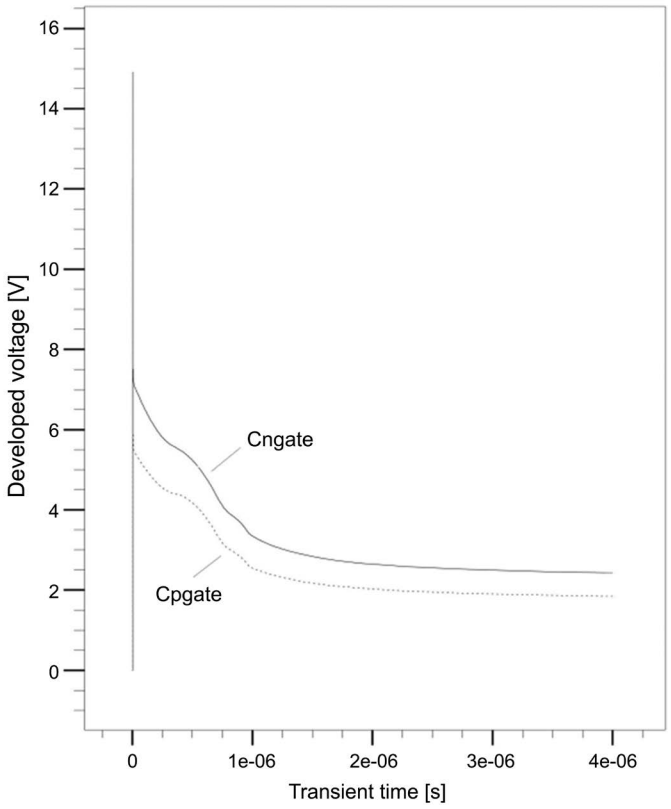

Figure 8. Variations of voltages on C_{ngate} and C_{pgate} in a PS mode discharge.

drops to 7.5 V within 2 ns, and main discharge proceeds. Compared to peaking up to 10.6 V during the main discharge duration when we use a 200 μm NMOS clamp device [6], it is a clear advantage. Since main discharge proceeds through the parasitic pnpn thyristors without any breakdown mode, the pad voltage decreases much faster compared to the case when using an NMOS clamp device [6], which is a clear improvement in the aspect of protecting gate oxides.

The voltage on C_{pgate} shown in **Figure 8** peaks up to 12.3 V for a very short duration, and drops to 5. The differences with respect to those on C_{ngate} are the voltage drops in the ESD diode connected between the pad and the V_{DD} bus.

From the same simulation result, we showed in **Figure 9** variation of overall peak temperature inside the protection devices including D_1, D_2, and D_3. Overall peak temperature increases up to 396˚K at 158 ns. This peak temperature is lower by 88˚K when compared to the case when using the NMOS clamp [6].

We confirmed that overall peak temperature appears at the p^+-subr and p^+-subl junctions inside D_2, not inside D_3 similarly as in case of using the NMOS clamp [6]. This peak temperature is determined by the cathode voltage of D_2 as explained in [6], which is 4.83 V at 158 ns and equal to the anode voltage of D_3.

We confirmed that peak temperature inside D_3 increases only up to 315˚K at 435ns, which appears around the Pa1/Dnw1/p-sub junction. Therefore it seems that there is a large room for reducing the size of D_3 smaller than 200 μm to reduce the DC V_{DD}-V_{SS} leakage.

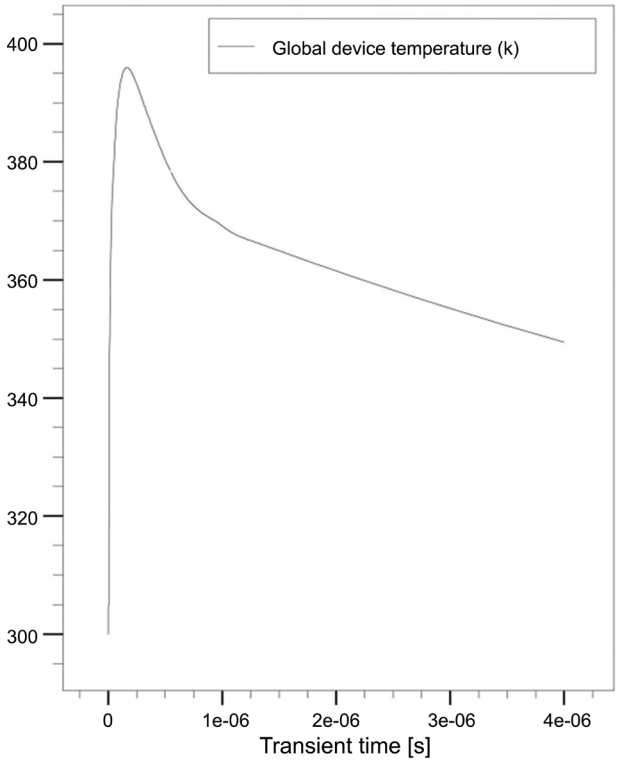

Figure 9. Overall peak temperature variation in a PS mode discharge.

5. Conclusions

Based on 2-D device simulations and mixed-mode transient simulations, we showed that pnpn thyristor action inside the diode string clamp dominates the PS-mode HBM discharge transient of a CMOS chip equipped with a diode ESD protection scheme utilizing a triple-well diode-string clamp.

We explain in detail the mechanisms involved in ESD discharge inside the diode-string clamp, which has never been done anywhere in the literature based on simulations or measurements.

Even though this work is based on simulations utilizing device and circuit simulators, the analysis given in this work clearly explain the mechanism involved, which cannot be done by measurements.

Contributions of this work can be summarized as follows.

1) We showed by DC simulations that there exists pnp bipolar transistor action leading to a sudden increase in the substrate leakage in a triple-well 4-diode string if the anode bias is getting high.

2) Through mixed-mode transient simulations for a 2000 V PS-mode HBM ESD discharge event, we showed that there exists a dominant discharge path formed by a parasitic pnpn thyristor and an npn bipolar transistor in series if we use the triple-well 4-diode string as a clamp device in a diode protection circuit.

3) Using the same simulation results, we showed that percentage of the current through the series-connected pnpn thyristor and an npn bipolar transistor in the 4-diode string clamp device is about 70%, and the current through the

series-connected 4-diode string is about 28%. Only 2% of the discharge current flows out through the p substrate terminal.

Acknowledgements

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