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Electronically-Controllable Grounded-Capacitor-Based Grounded and Floating Inductance Simulated Circuits Using VD-DIBAs

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ABSTRACT

New Voltage Differencing Differential Input Buffered Amplifier (VD-DIBA) based lossless grounded and floating inductance simulation circuits have been proposed. The proposed grounded simulated inductance circuit employs a single VD-DIBA, one floating resistance and one grounded capacitor. The floating simulated inductance (FI) circuits employ two VD-DIBAs with two passive components (one floating resistance and one grounded capacitor). The circuit for grounded inductance does not require any realization conditions where as in case of floating inductance circuits, a single matching condition is needed. Simulation results demonstrating the applications of the new simulated inductors using CMOS VD-DIBAs have been included to confirm the workability of the new circuits.

Keywords: VD-DIBA; Inductance Simulation; Filters

1. Introduction

The importance of grounded and floating simulated inductors in the context of active network synthesis is well known [1]. Several grounded and floating inductance simulation schemes, employing different active elements such as operational amplifiers (op-amps) [2-6], current conveyors (CCs) [7-15], current controlled conveyors (CCCIIs) [16,17], current feedback operational amplifiers (CFOAs) [18,19], operational mirrored amplifiers (OMAs) [20], differential voltage current conveyors (DVCCIIs) [21], current differencing buffered amplifiers (CDBAs) [22,23], current differencing transconductance amplifiers (CDTAs) [24,25], operational transconductance amplifiers (OTAs) [26,27] have been reported in the literature. In [28], many new active building blocks have been introduced; VD-DIBA is one of them. Till now, some applications of VD-DIBAs have been reported in the open literature such as in the realization of all pass filters [29], realization of grounded and floating inductance circuits using two/three VD-DIBAs as reported in [30], electronically controllable sinusoidal oscillator in [31] and voltage-mode universal biquad in [32,33]. The purpose of this paper is to introduce new VD-DIBA-based: 1) a lossless grounded inductor using only a single VD-DIBA, one resistor and a grounded capacitor without requiring any matching condition and 2) two floating inductance simulation circuits employing two VD-DIBAs, one resistor and a grounded capacitor along with a single matching condition for floatation. The genesis of these FI circuits is inspired by [1,34,35].

2. The Proposed New Configuration

The schematic symbol and equivalent model of the VD-DIBA (−) are shown in **Figures 1(a)** and **(b)** respectively [29]. The model of VD-DIBA (−) includes two controlled sources: the current source controlled by differential voltage $\left(V_+ - V_-\right)$, with the transconductance g_m, and the voltage source controlled by differential voltage $\left(-V_z + V_v\right)$, with the unity voltage gain. The VD-DIBA (−) can be described by the following set of equations:

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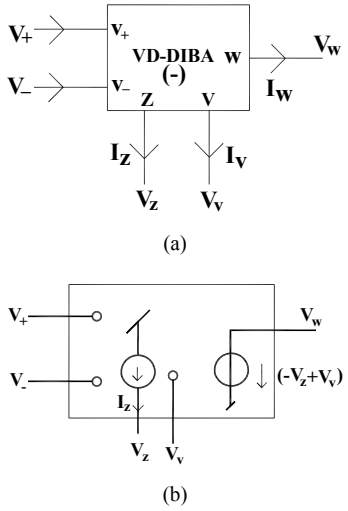


Figure 1. (a) Schematic symbol (b) equivalent model of VD-DIBA.

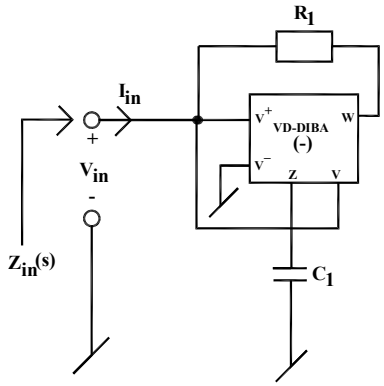


Figure 2. Proposed grounded inductance simulation configuration.

$$\begin{pmatrix} I_+ \\ I_- \\ I_z \\ I_v \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_v \\ I_w \end{pmatrix} \quad (1)$$

The proposed grounded and floating inductance circuits are shown in **Figure 2** and **Figure 3** respectively.

A routine analysis of the circuit shown in **Figure 2** results in the following expression for the input impedance

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = s\left(\frac{C_1 R_1}{g_m}\right) \quad (2)$$

The circuit, thus, simulates a grounded inductance with the inductance value given by

$$L_{eq} = \frac{C_1 R_1}{g_m} \quad (3)$$

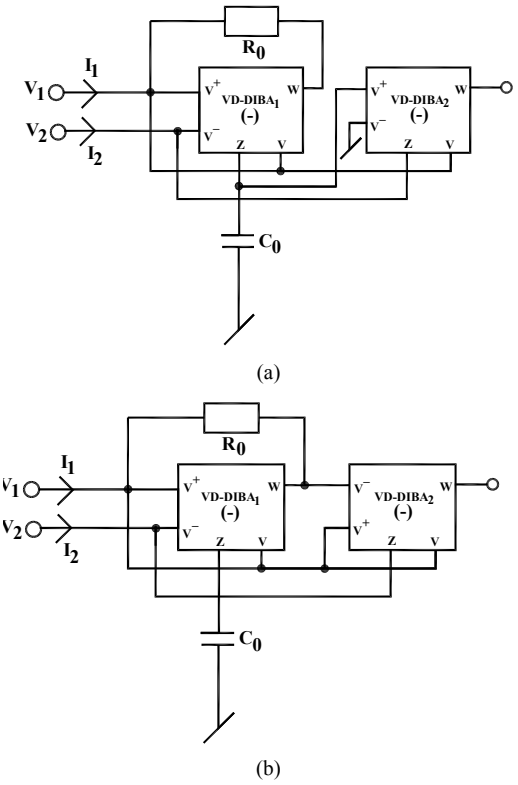


Figure 3. Proposed floating inductance simulation configurations.

On the other hand, analysis of the new FI circuits shown in **Figures 3(a)** and **(b)** yields

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{sC_0} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \text{ with } g_{m_2} = \frac{1}{R_0} \quad (4)$$

which proves that the circuits simulate a floating lossless inductance with the inductance value given by

$$L_{eq} = \frac{C_0}{g_{m_1} g_{m_2}} \quad (5)$$

The proposed CMOS implementation of VD-DIBA (−) is shown in **Figure 4**. The CMOS VD-DIBA (−) is implemented using 0.35 μm MIETEC real transistor model which are listed in **Table 1**. Aspect ratios of transistors used are given in **Table 2**.

3. Non-Ideal Analysis and Sensitivity Performance

Let R_z and C_z denote the parasitic resistance and parasitic capacitance of the Z-terminal. Taking into account the non-idealities of the VD-DIBA (−), namely $V_w = \left(-\beta^+ V_z + \beta^- V_v\right)$, where $\beta^+ = 1 - \varepsilon_1 \left(\varepsilon_1 \ll 1\right)$ and $\beta^- = 1 - \varepsilon_2 \left(\varepsilon_2 \ll 1\right)$ are voltage tracking errors of the VD-DIBA, for the circuit shown in **Figure 2**, the non-ideal input impedance is found to be

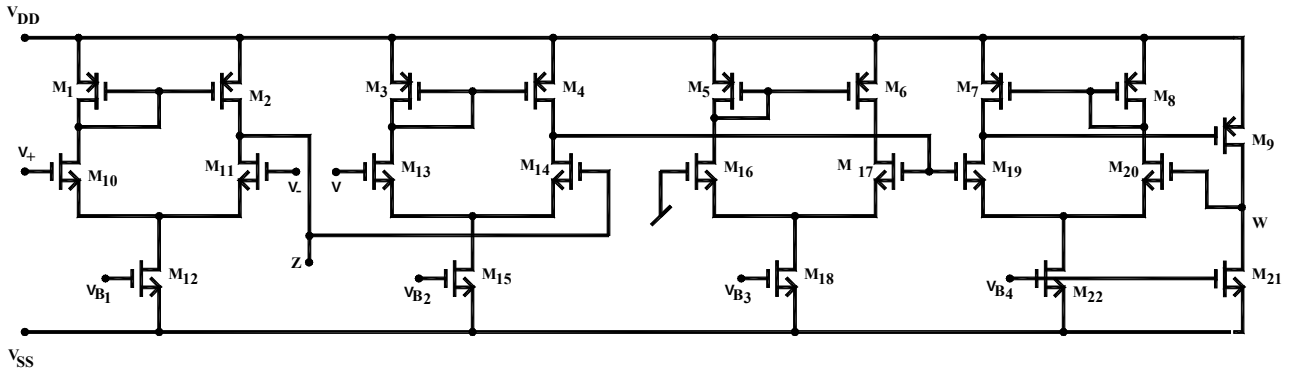


Figure 4. Proposed CMOS Implementation of VD-DIBA, $V_{DD} = -V_{SS} = 2$ V, $V_{B1} = -0.44$ V, $V_{B2} = I_{B3} = -0.22$ V and $V_{B4} = -0.9$ V.

Table 1. CMOS process parameters.

	N MOS	P MOS
LEVEL	3	3
TOX	7.9E-9	7.9E-9
NSUB	1E17	1E17
GAMMA	0.5827871	0.4083894
PHI	0.7	0.7
VTO	0.5445549	-0.7140674
DELTA	0	0
UO	436.256147	212.2319801
ETA	0	9.999762E-4
THETA	0.1749684	0.2020774
KP	2.055786E-4	6.733755E-5
VMAX	8.309444E4	1.181551E5
KAPPA	0.2574081	1.5
RSH	0.0559398	30.0712458
NFS	1E12	1E12
TPG	1	−1
XJ	3E-7	2E-7
LD	3.162278E-11	5.000001E-13
WD	7.046724E-8	1.249872E-7
CGDO	2.82E-10	3.09E-10
CGSO	2.82E-10	3.09E-10
CGBO	1E-10	1E-10
CJ	1E-3	1.419508E-3
PB	0.9758533	0.8152753
MJ	0.3448504	0.5
CJSW	3.777852E-10	4.813504E-10
MJSW	0.350872	0.5

Table 2. Dimensions of CMOS transistors.

Transistor	W/L (μm)
M1-M6	14/1
M7-M9	14/0.35
M10-M18	4/1
M19-M22	7/0.35

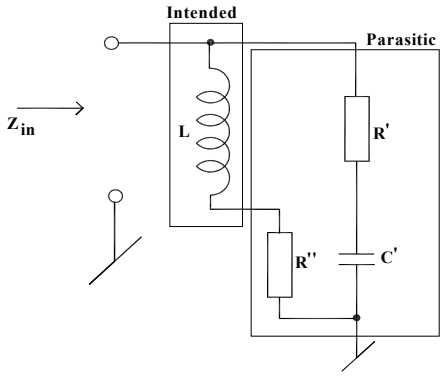


Figure 5. Non-ideal equivalent circuit of grounded inductor of Figure 2.

$$Z_{in}(s) = \frac{\left\{ s\left(C_1 + C_z\right) + \frac{1}{R_z} \right\}}{\left\{ s\frac{\left(C_1 + C_Z\right)\left(1-\beta^-\right)}{R_1} + \frac{\left(1-\beta^-\right)}{R_1 R_Z} + \frac{\beta^+ g_m}{R_1} \right\}} \tag{6}$$

From the above, a non-ideal equivalent circuit of the grounded inductor is derivable which is shown in **Figure 5**.

Where $L = \frac{\left(C_1 + C_z\right) R_1 R_Z}{\left\{\left(1-\beta^-\right) + \beta^+ g_m R_Z\right\}}$, $R' = \frac{R_1}{\left(1-\beta^-\right)}$,

$C' = \frac{\left(C_1 + C_Z\right)\left(1-\beta^-\right) R_Z}{R_1}$,

and $R'' = \dfrac{R_1}{\left\{\left(1-\beta^-\right)+\beta^+ g_m R_Z\right\}}$

From the above, the sensitivities of L with respect to various active and passive elements are found to be

$$S_{C_0}^L = \frac{C_1}{(C_1+C_z)}, S_{C_z}^L = \frac{C_z}{(C_1+C_z)}, S_{R_0}^L = 1,$$
$$S_{R_z}^L = \frac{\left(1-\beta^-\right)}{\left\{\left(1-\beta^-\right)+\beta^+ g_m R_Z\right\}},$$
$$S_{\beta^-}^L = \frac{\beta^-}{\left\{\left(1-\beta^-\right)+\beta^+ g_m R_Z\right\}}, \quad (7)$$
$$S_{\beta^+}^L = -\frac{\beta^+ g_m R_Z}{\left\{\left(1-\beta^-\right)+\beta^+ g_m R_Z\right\}},$$
$$S_{g_m}^L = -\frac{\beta^+ g_m R_Z}{\left\{\left(1-\beta^-\right)+\beta^+ g_m R_Z\right\}}$$

similarly, for the circuit shown in **Figures 3(a)** and **(b)** for $\beta^- = \beta^+ = 1$, the input-output currents and voltages relationships are given by:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{\left\{s\left(C_0 + C_{z_1}\right) + \dfrac{1}{R_{Z_1}}\right\}} \times \begin{bmatrix} 1 & -1 \\ -1 & 1 + \dfrac{\left\{s\left(C_0 + C_{z_1}\right) + \dfrac{1}{R_{Z_1}}\right\}\left(sC_{z_2} + \dfrac{1}{R_{Z_2}}\right)}{g_{m_1} g_{m_2}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

with $g_{m_2} = \dfrac{1}{R_0}$ (8)

The non-ideal equivalent circuit of floating inductors of **Figures 3(a)** and **(b)** derivable from Equation (8) is shown in **Figure 6**.

Where $L = \dfrac{\left(C_0 + Cz_1\right)}{g_{m_1} g_{m_2}}$ and $R = \dfrac{1}{R_{z_1} g_{m_1} g_{m_2}}$

The various sensitivities of L with respect to active and passive elements are:

$$S_{C_0}^L = \frac{C_0}{\left(C_0 + C_{z_1}\right)}, S_{C_{z_1}}^L = \frac{C_{z_1}}{\left(C_0 + C_{z_1}\right)}, S_{g_{m_1}}^L = -1,$$
$$S_{g_{m_2}}^L = -1,\ S_{\beta^+}^L = 0,\ S_{\beta^-}^L = 0 \quad (9)$$

Taking $g_{m_1} = g_{m_2} = 389.673\ \mu\text{A/V}$, $C_{z_1} = C_{z_2} = 0$, $R_{z_1} = R_{z_2} = \infty$, $C_0 = 0.1\ \text{nF}$ and $R_0 = 100\ \text{k}\Omega$, these sensitivities are found to be (1, 0, 1, 0, 0, −1) and (1, 0, −1, −1, 0, 0) for Equations (7) and (9) respectively. Thus,

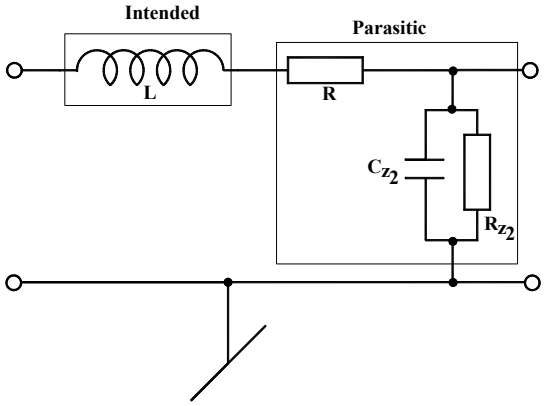


Figure 6. Non-ideal equivalent circuit of floating inductor of Figure 3.

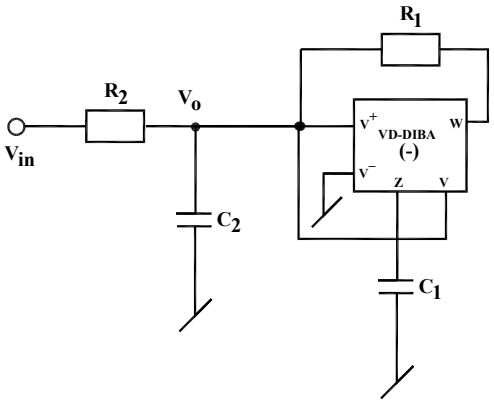


Figure 7. Band pass filter realized by the new grounded simulated inductor.

all the passive and active sensitivities of both grounded and floating inductance circuits are low.

4. Simulation Results of the New Proposed Grounded/Floating Inductance Configurations

The workability of the proposed simulated inductors has been verified by realizing a band pass filter (BPF) as shown in **Figures 7** and **8**.

The transfer function realized by this configuration is given by

$$\frac{V_0}{V_{in}} = \frac{s\left(\dfrac{1}{R_2 C_2}\right)}{s^2 + s\left(\dfrac{1}{R_2 C_2}\right) + \left(\dfrac{g_{m_1}}{C_1 C_2 R_1}\right)} \quad (10)$$

from where it is seen that bandwidth and centre frequency are independently tunable, the former by R_2 and the latter by any of R_1, g_{m_1} and C_1.

The transfer function realized by configuration shown in **Figure 8** is given by

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{R_1 g_{m_1} g_{m_2}}{C_0}\right)}{s^2 + s\left(\frac{R_1 g_{m_1} g_{m_2}}{C_0}\right) + \frac{g_{m_1} g_{m_2}}{C_0 C_1}} \text{ with } g_{m_2} = \frac{1}{R_0}, \tag{11}$$

In this case, bandwidth is tunable by R_1 whereas centre frequency can be tuned by C_1.

Performance of the new simulated inductors was verified by SPICE simulations. CMOS-based VD-DIBA (−) (as shown in **Figure 4**) was used to determine the frequency responses of the grounded and floating simulated inductors. The following values were used for grounded inductor: $C_1 = 0.01$nF, $R_1 = 100$ kΩ, $g_{m_1} = 296.468\ \mu A/V$ and for the floating inductor: $C_0 = 0.01$ nF, $R_0 = 100$ kΩ, $g_{m_1} = 296.468\ \mu A/V$, $g_{m_2} = 10\ \mu A/V$. From the frequency response of the simulated grounded inductor (**Figure 9**) it has been observed that the inductance value remains constant up to 1 MHz. Similarly, from the frequency response of the simulated floating inductor (**Figure 10**) the inductance value also remains constant up to 1 MHz.

To verify the theoretical analysis of the application circuits shown in **Figures 7** and **8**, they have also been simulated using CMOS-based VD-DIBA (−) as shown in **Figure 4**. The component values used were for **Figure 7**: $C_1 = 0.1$ nF, $C_2 = 1$ pF, $R_1 = 100$ kΩ, $R_2 = 113.258$ kΩ and for **Figures 8(a)** and **(b)**: $C_0 = 0.1$ nF, $C_1 = 0.01$ nF, $R_0 = 100$ kΩ, $R_1 = 71.652$ kΩ, $g_{m_2} = 10\ \mu A/V$ (which can be maintained by taking $V_{B1} = -1.5$V). The VD-DIBA was biased with ±2 volts D.C. power supplies with $V_{B1} = -0.44$V, $V_{B2} = V_{B3} = -0.22$V and $V_{B4} = -0.9$V. VD-DIBA (−) transconductance is controlled by V_{B1}. **Figure 11**, **Figures 12(a)** and **(b)** show the simulated filter responses of the BP filters.

The above described results, thus, confirm the validity of the application of the proposed grounded and floating simulated inductance circuits. A comparison of the various salient features of the proposed configurations as compared to other previously known grounded and FI

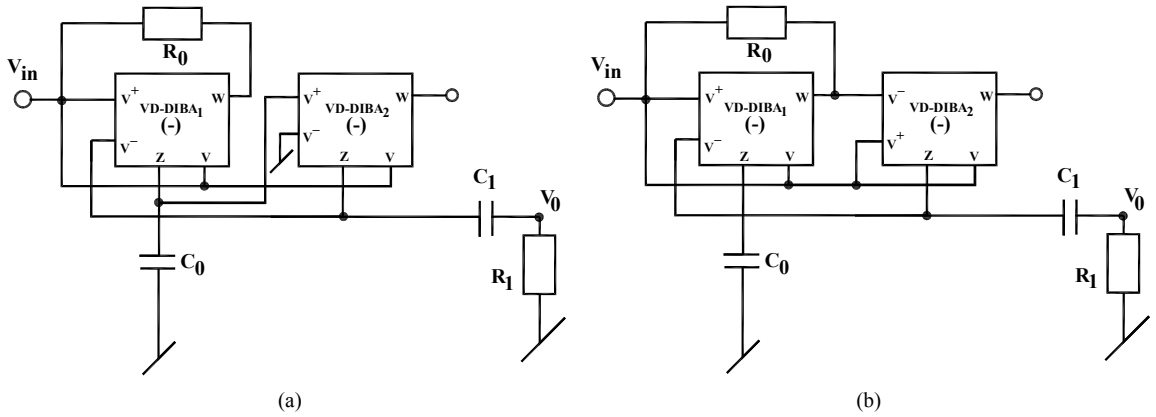


Figure 8. Band pass filters realized by the new floating simulated inductors of Figures 3(a) and (b).

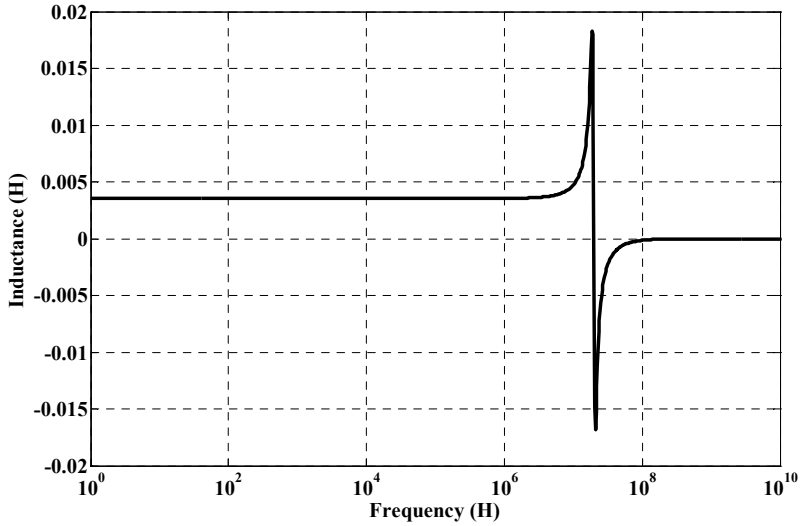


Figure 9. Frequency response of the simulated grounded inductor.

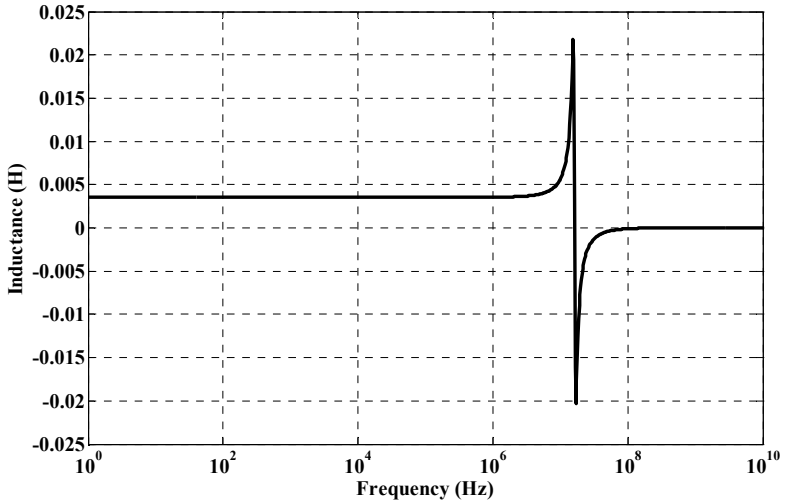


Figure 10. Frequency response of the simulated floating inductor.

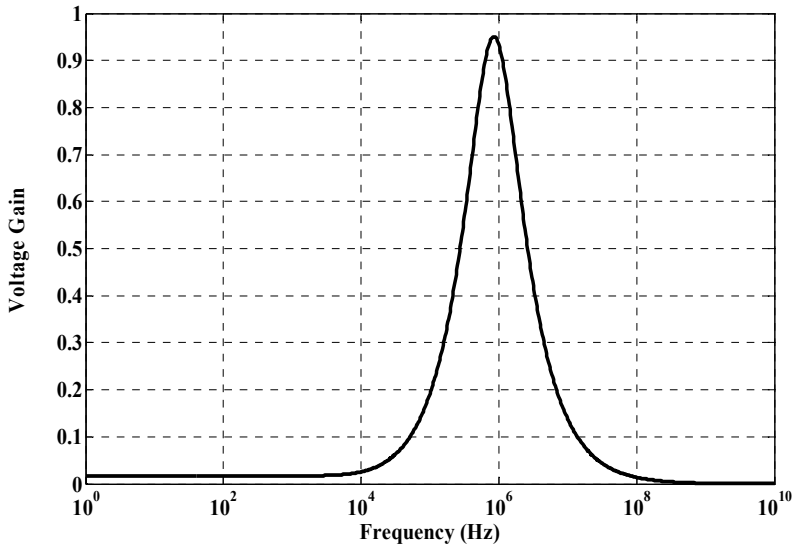
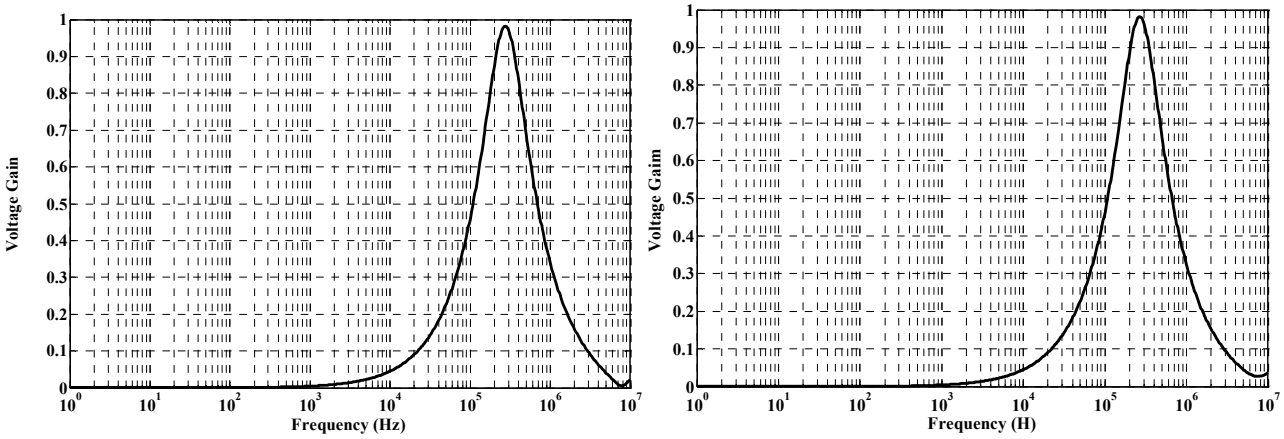


Figure 11. Frequency response of BPF using the proposed simulated grounded inductor.



(a) (b)

Figure 12. Frequency response of BPF using the proposed simulated floating inductor.

Table 3. Comparison with other previously published grounded and floating inductors.

Reference	Inductance type*	Number of active elements used	Number of resistors used	Number of capacitors used	Matching condition required	Availability of Electronic tunability
[4]	F	3	3	1	yes	no
[7]	F	3/2	2	1	no	no
[8]	F	4	4	1	yes	no
[9]	F	4	3	1	yes	no
[10]	F	4	2	1	no	no
[11]	F	4	2	1	no	no
[12]	F	2	2	1	no	no
[14]	G	1	2	1	yes	no
[16]	F	4/3	3	1	no	no
[17]	G	2	0	1	no	yes
[18]	G	2	2	1	no	no
[19]	F	2	3	2	yes	no
[20]	F	3	2	1	no	no
[21]	G	3	4	1	no	no
	F	3	4	1	no	no
[22]	F	3/4	4	1	yes	yes
[23]	F	3	0	1	yes	yes
[24]	F	3	0	1	yes	yes
[25]	G	2	0	1	no	yes
	F	3	0	1	yes	yes
[26]	G	2	0	1	no	yes
	F	3	0	1	yes	yes
[30]	G	2	0	1	no	yes
	F	3	0	1	yes	yes
[36]	F	3	2	1	no	no
[37]	G	3	3	1	no	no
Proposed	G	1	1	1	no	yes
	F	2	1	1	yes	yes

*F = Floating, G = Grounded.

simulators has been included in **Table 3**.

5. Conclusions

New circuits of lossless grounded and floating inductance have been proposed employing VD-DIBAs. The proposed grounded inductance circuit employs only one VD-DIBA (−), one resistor and one grounded capacitor and does not require any component matching condition. On the other hand, the two floating inductance configurations each using two VD-DIBAs (−), one resistor and one grounded capacitor, need only a single realization condition for floatation. The SPICE simulation results have confirmed the workability of the new propositions as well as the suggested application examples using them.

The problem of realizing any new single VD-DI-BA-based FI configuration using a single grounded capacitor and without requiring any matching condition appears to be an interesting problem which is open to be investigated.

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