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Analytical and Numerical Model Confrontation for Transfer Impedance Extraction in Three-Dimensional Radio Frequency Circuits

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ABSTRACT

3D chip stacking is considered known to overcome conventional 2D-IC issues, using through silicon vias to ensure vertical signal transmission. From any point source, embedded or not, we calculate the impedance spread out; our ultimate goal will to study substrate noise via impedance field method. For this, our approach is twofold: a compact Green function or a Transmission Line Model over a multi-layered substrate is derived by solving Poisson's equation analytically. The Discrete Cosine Transform (DCT) and its variations are used for rapid evaluation. Using this technique, the substrate coupling and loss in IC's can be analyzed. We implement our algorithm in MATLAB; it permits to extract impedances between any pair of embedded contacts. Comparisons are performed using finite element methods.

Keywords: Through Silicon Via (TSV); Green's Function; Transmission Line Model; Radio Frequency (RF); Transfer Impedance Extraction

1. Introduction

As the complexity of mixed digital-analog designs increases and the area of the current technologies decreases, substrate noise coupling in integrated circuits becomes a significant consideration in the design. Nowadays, nanotechnology and the development of semiconductor technology enable designers to integrate multiple systems into a single chip, not only in 2D (planar), but also in 3D (in the bulk). This design technology reduces cost, while improves performance and makes the system on chip possible. Through Silicon Vias (TSV) or through wafer interconnection is most likely the solution to go to 3D device stacking [1-3]. The potential benefits of 3D integration can vary depending on approach; they include multifunctionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs. A key study in a recent paper of ourselves [4] comes from the fact that, when, for instance, the MOS bulk-electrode is floating, the bulk potential becomes a function of the substrate perturbations and this affects, for instance, the value of the MOS threshold voltage which in turn varies the MOS drain current. Also, the switching of the MOS drain current due to an applied square signal is a strong function of the MOS and the bulk capacitances. So, our aim was to de- termine the source of the bulk variation: the CMOS input voltage or the TSV HV (High Voltage: ~42 V) signal and hence evaluate the impact of the TSV on the CMOS inverter (**Figure 1**). The CMOS devices are implemented using the standard layers of the 0.35 µm BiCMOS ST Microelectronics-like technology and with threshold voltages of 0.65 V for nMOS and –0.6 V for pMOS.

2. CMOS Compact Model

To achieve this aim, basic simulations are performed using the SPICE models for the CMOS devices, the finite element method (FEM) for the bulk regions of the devices, and this mixed-mode simulation is performed using TCAD program packages. In the mixed mode simulation, we use the SPICE model parameters which are extracted by means of the ICCAP RF extraction program [5]. In this section the technological process steps of the CMOS in 0.35 µm BiCMOS technology is presented.

We start up with a lightly-doped P-type wafer (2E 15 cm^3) and form the buried N^+ layer by ion implantation of

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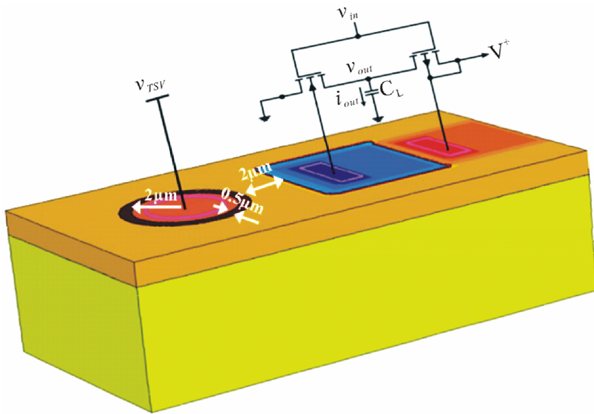

Figure 1. 3D cross-section of TSV-CMOS mixed mode coupling.

arsenic into the respective mask pattern. Afterwards, a high temperature anneal is performed to remove damage defects and to diffuse the arsenic into the substrate. During this anneal an oxide is grown in the buried N^+ windows to provide a silicon step for alignment of subsequent levels. Therefore, the nitride mask is selectively removed and the remaining oxide serves as blocking mask for the buried P^+ layer implant. After finishing the alignment of the buried layer and the deposition of the epitaxial-layer a twin well process is used to fabricate the N-well of the pMOS and the P-well of the nMOS. As compared to conventional CMOS a relatively short well drive-in (100 min) is performed at 1150˚C. After the wells are fabricated, the whole wafer is planarized and a pad oxide is grown. The oxide is capped with a thick nitride. After patterning the active regions of the devices, an etch step is used to open up the field isolation regions. Prior to field oxidation, a blanket channel stop is implanted. Oxidation is used to fabricate a 300 nm thick field oxide. To minimize buried layer diffusion, the oxidation temperature is quite moderate (900˚C). Then the nitride masks are removed from the active regions. We proceed with the resist strip and perform a pre-gate oxide etch to clean the oxide surface. A 7.6 nm thick gate oxide is grown on top. Then a polycrystalline silicon layer is deposited. This polysilicon layer is implanted with arsenic for the nMOS and boron for the pMOS; the dopants will diffuse out from the polysilicon layer at the final source-drain anneal. The polysilicon layer is patterned to define the CMOS gates. Phosphorus and boron are implanted to form shallow LDD regions for the nMOS and pMOS devices. Then the sidewall spacer formation is initiated. Therefore, an oxide layer is deposited and anisotropically etched back. Next, the source-drain regions are heavily doped by phosphorus and boron, which is depicted. Finally, the fabrication of the active regions is finished by the source-drain anneal. Hence, a 30 s long RTA anneal at 850˚C is performed.

The schematic cross-section of the CMOS including the active area doping concentrations is shown in the **Figure 2**. The retrograde well utilizes high-energy implant to produce a self-aligned channel stop and an extremely shallow, low sheet-resistance while maintaining controllable, low channel threshold voltages. It shunts the vertical device which is the key to successfully harnessing the parasitic vertical bipolar transistor. Short channel effects can be minimized by increasing the background doping concentration and decreasing the gate oxide thickness. Shallow source/drain (≈0.2 µm) is used to reduce short channel effects and overlap capacitance. The hot carrier effects are controlled by introducing the lightly-doped drains (LDD). In the light of the above mentioned technological steps, the simulated CMOS 2D cross-section is shown in **Figure 3** and the technological process steps are summarized in **Figure 4**. Extracted from typical characteristics (**Figure 5**) compact model electrical parameters for NMOS and PMOS are shown in **Table 1** (using LEVEL3 SPICE model). As an example, a 2D structure is shown in **Figure 6(a)**, with the TSV placed near the nMOS device with T_{OXTSV} = 0.5 µm and V^+ = 1.2 V. In this structure, the pMOS bulk and source electrodes are shorted and only the impact on the nMOS

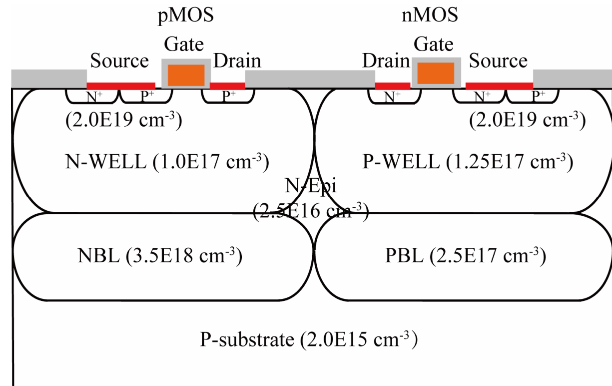

Figure 2. The schematic cross-section of the CMOS.

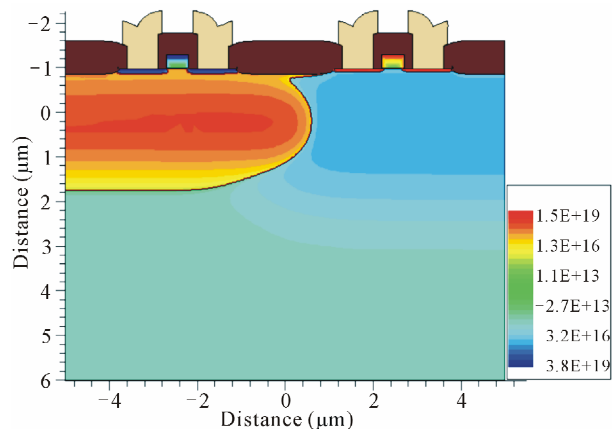

Figure 3. 2D cross-section of CMOS.

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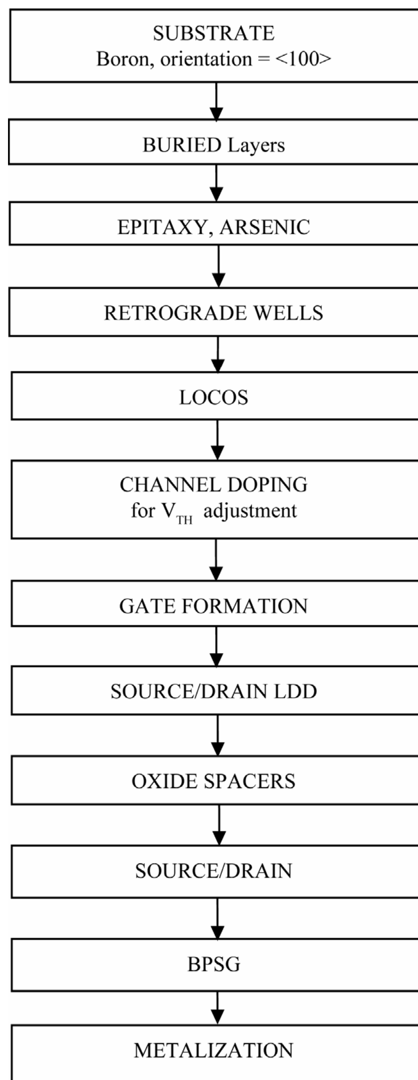

Figure 4. The process steps of a 0.35 µm BiCMOS technology.

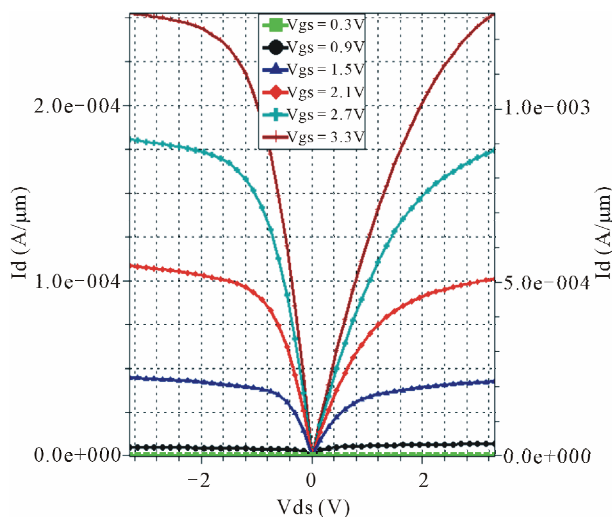

Figure 5. nMOS and pMOS; e.g. Id-Vd$_S$ characteristics.

Table 1. The SPICE model parameters of CMOS devices.

model nMOS (LEVEL = 3)	model pMOS (LEVEL 3)
+UO = 5.829856E+02	+UO = 95.7
+VTO = 5.362076E–01	+VTO = –5.593849E–01
+TOX = 7.600 n	+TOX = 7.600 n
+NSUB = 1.5E+17	+NSUB = 1.00E+17
+VMAX = 2.854458E+05	+VMAX = 3.067345E+04
+CJ = 5.0E–04	+CJ = 100.6 u
+MJ = 0.5	+MJ = 500.5 m
+CJSW = 5.0E–10	+CJSW = 50.30 p
+MJSW = 0.33	+MJSW = 500.5 m
+CGDO = 6.0E–09	+CGDO = 8.0E–09
+CGSO = 6.0E–09	+CGSO = 8.0E–09
+CGBO = 6.0E–09	+CGBO = 8.0E–09
+PB = 1	+PB = 982.3 m
+FC = 0.5	+FC = 500.0 m
+XJ = 200 n	+XJ = 200.00 n
+DELTA= 2.255185E–02	+DELTA = 3.291260E–02
+THETA = 0.08	+THETA = 36.9 m
+ETA = 0	+ETA = 100.0 m
+KAPPA = 0.6)	+KAPPA = 0.01)

is supposed as shown in **Figure 6(a)**. The potential distribution in the TSV-CMOS structure is shown in **Figure 6(a)**; it is clearly observed that nearly half of the TSV voltage is dropped across the TSV oxide (at the left) and the other half across the depleted region in the substrate and there is a few potential contours are observed in the active regions of the MOS devices. The waveforms of the TSV, CMOS input and output voltages and the output current wave form (the current through the load capacitor) are shown in **Figure 6(b)**. It is cleared from the figure that the current is switching w.r.t the CMOS input waveform and there is no effect of the digital HV signal of the TSV.

In order to accelerate the devices and circuit design without significant loss of accuracy and reliability, designer should not model the substrate with numerical methods.

Especially in the high-frequency cases, the loss of the circuit performance caused by the silicon substrate is very important. Considering the radio frequency (RF) range, the substrate could have, at some nodes of interest, an "RLC" behavior (approximately an "RC" one for low frequencies); it is important to prevent the whole system

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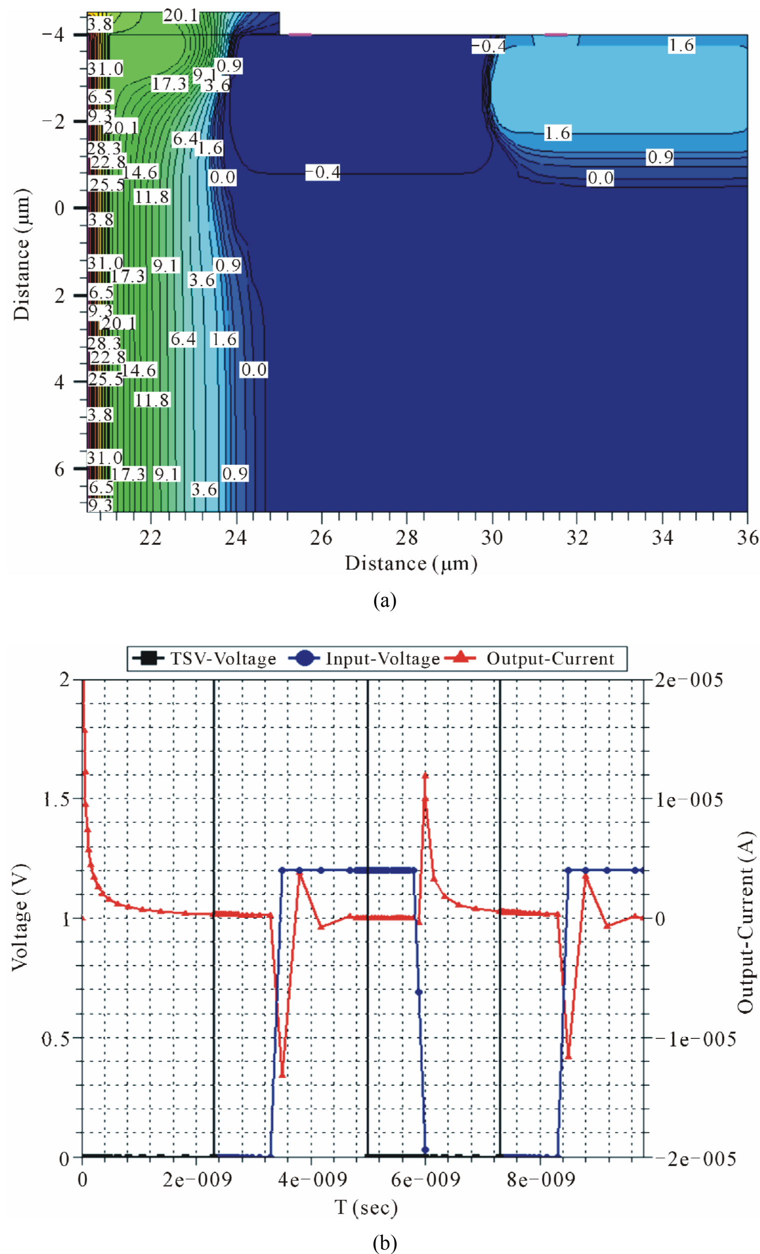

Figure 6. (a) The Potential distribution, and (b) the voltages and output-current waveforms for V_{in} = 0.0/1.2 V and V_{TSV} = 0.0/42.0 V.

(die, with its packaging) from surges, bounces, or parasitic oscillations. So we need effective tools to analyze the practical layout, to calculate the electric performance of the circuit. We need calculate the impedance matrix and partial inductance matrix to analyze the substrate coupling.

Here, Green function will be applied for homogeneous layers to the substrate circuit model extraction, as opposed to numerical method; the resolution speed of this method is much faster. Some basic recalls and concept are first introduced. The use of discrete cosine transforms (DCT) or Fast Fourier transforms (FFT) in this model will accelerate the compute speed obviously. Then an improved model which can be applied on substrate with in-depth contacts is shown; it can treat the case of contacts lying in different layers. As a check, we compare with a FEM method [6].

3. Substrate Extraction

3.1. Green Kernels

In this paragraph, we present a technique for modeling the substrate. This algorithm relies on the electrostatic Green function in the substrate medium and the Fast

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Fourier Transform; it is well known when contacts are on the die surface [7,8].

Green Function and Poisson's Equation [9,10]
Posing and solving problems that are described by the Poisson equation is one of the cornerstones of electrostatics. Poisson's equation is handled as:

$$\Delta V = -\frac{\rho}{\varepsilon} \quad (1)$$

where, V is the electrical potential, ρ is the charge density and ε the dielectric permittivity of the medium.

The algorithm is the same for the electrostatic or quasi-static case where Poisson's equation is replaced by the Ohm's Law (neglecting the diffusion currents):

$$\boldsymbol{J} = \sigma \cdot \boldsymbol{E}, \quad (2)$$

with $\sigma = \sigma_0 + j\omega\varepsilon$, for the harmonic domain.

Where, J is the current density in $\text{A}\cdot\text{m}^{-2}$, E the electric field in $\text{V}\cdot\text{m}^{-1}$ and σ the conductivity of the medium in $\text{S}\cdot\text{m}^{-1}$. A different form of the law's ohm is given by:

$$\Delta V = -\frac{\text{div}(\boldsymbol{J})}{\sigma}, \quad (3)$$

where V is the potential (V), div(J) is not null since an extent current (density) is imposed.

Finding V for some given $\rho(=1/\sigma)$ and ε is an important practical problem, since this is the usual way to derive the electric potential for a given charge distribution.

The above equation may be turned into an integral equation of the form:

$$\phi(r) = \int_V \rho(r') G(r, r') \mathrm{d}^3 r' \quad (4)$$

G is the potential due to a point charge placed at a point r' and G is known as Green function (or Kernel).

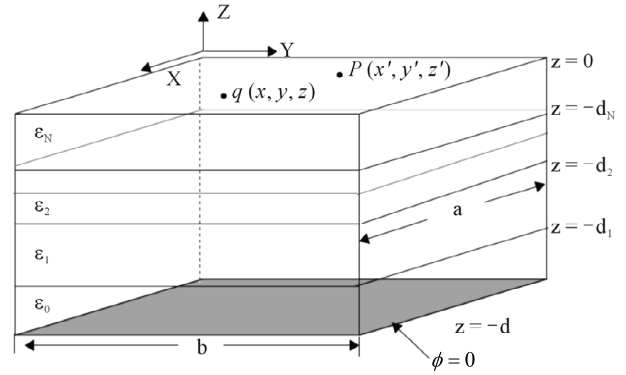
The Green function can be got by solving the following equation:

$$\nabla^2 G = -\frac{\delta(r - r')}{\varepsilon} \quad (5)$$

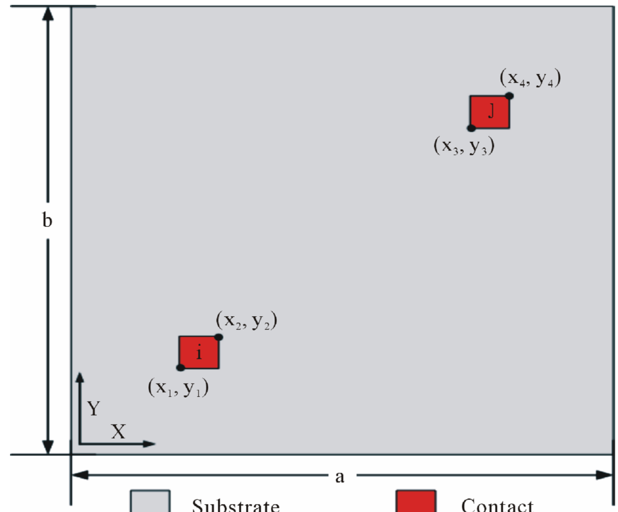
If the Green function is known, this equation does provide a technique for determining the potential at any point in the volume V due to a known arbitrarily distributed charge density.

Consider a localized charge at the point P (x', y', z') in the upper layer of stacked dielectric layers as shown on the **Figure 7(a)**. Here, we assume the substrate as an equivalent system composed of stacked layers; each of them has a dielectric constant and a resistivity of the corresponding resistive substrate layer.

The potential in Q (x, y, z) induced by the charge in P is the solution of Poisson's equation and is given by:



(a)



(b)

Figure 7. (a) Stacked layers model of the substrate and (b) Top view: contact altitudes: –d < z_i, z_j < 0.

$$\Delta G(x, y, z, x', y', z') = -\frac{\delta(x - x') \cdot \delta(y - y') \cdot \delta(z - z')}{\varepsilon_N} \quad (6)$$

If we assume that $G = X(x, x').\ Y(y, y').\ Z(z, z')$, we can rewrite the Poisson's equation, thus resulting in:

$$Y \cdot Z \cdot \frac{\mathrm{d}^2 X}{\mathrm{d}x^2} + X \cdot Z \cdot \frac{\mathrm{d}^2 Y}{\mathrm{d}y^2} + X \cdot Y \cdot \frac{\mathrm{d}^2 Z}{\mathrm{d}z^2} = -\frac{\delta(x - x') \cdot \delta(y - y') \cdot \delta(z - z')}{\varepsilon_N} \quad (7)$$

Noting a and b the die dimensions, we get:

$$X = \cos\left(\frac{m \cdot \pi \cdot x}{a}\right);\ Y = \cos\left(\frac{n \cdot \pi \cdot y}{b}\right) \quad \text{with } m \in [0, \infty) \text{ and } n \in [0, \infty) \quad (8)$$

(m and n are integers)

The Green's function-equation-involves an infinite series of sinusoidal functions:

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$$\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\cos\left(\frac{m\cdot\pi\cdot x}{a}\right)\cdot\cos\left(\frac{n\cdot\pi\cdot y}{b}\right)\times\left[\frac{\mathrm{d}^2Z}{\mathrm{d}z^2}-\left(\left(\frac{m\cdot\pi\cdot x}{a}\right)^2+\left(\frac{n\cdot\pi\cdot y}{b}\right)^2\right)\cdot Z\right]=-\frac{\delta(x-x')\cdot\delta(y-y')\cdot\delta(z-z')}{\varepsilon_N} \quad (9)$$

By defining:

$$Z(z,z')=Z'(z,z')\cdot\cos\left(\frac{m\cdot\pi\cdot x'}{a}\right)\cdot\cos\left(\frac{n\cdot\pi\cdot y'}{b}\right) \quad (10)$$

we get a simple equation:

$$\frac{a\cdot b}{4}\cdot\left[\frac{\mathrm{d}^2Z}{\mathrm{d}z^2}-\gamma_{mn}^2\cdot Z\right]=-\frac{\delta(z-z')}{\varepsilon_N} \quad (11)$$

with $\gamma_{mn}=\sqrt{\left(\frac{m\cdot\pi\cdot x}{a}\right)^2+\left(\frac{n\cdot\pi\cdot y}{b}\right)^2}$.

For $z\neq z'$, $\delta(z-z')=0$. The above equation has the well known general solution:

$$Z'=A\cdot e^{-\gamma_{mn}\cdot(d+z)}+B\cdot e^{\gamma_{mn}\cdot(d+z)} \quad (12)$$

This equation invokes a transmitted wave and a reflected one. Then, after deriving formal mathematical solution for Equation (12), with boundary conditions, we will discuss hereafter on a more physical approach of the problem, using the so-called Transmission Lines Method (TLM).

A general solution, for $m > 0$ and $n > 0$ of the Green electrostatic function is given as:

$$\boldsymbol{G}(x,x',y,y',z,z')=\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left[\frac{2\cdot\left(A_N\cdot e^{-\gamma_{mn}\cdot(d+z_l)}+B_N\cdot e^{\gamma_{mn}\cdot(d+z_l)}\right)\cdot\left(e^{-\gamma_{mn}\cdot z_h}+e^{\gamma_{mn}\cdot z_h}\right)}{a\cdot b\cdot\varepsilon_N\cdot\gamma_{mn}\cdot\left(B_N\cdot e^{\gamma.d}-A_N\cdot e^{-\gamma.d}\right)}\right]\cdot\cos\left(\frac{m\cdot\pi\cdot x}{a}\right)\cdot\cos\left(\frac{n\cdot\pi\cdot y}{b}\right) \quad (13)$$

Then we can get, or instance, the expression of the capacities from the matrix of capacitive coefficients [***C***] by using this equation. In order to have [***C***] or [***G***] (conductance matrix), we only have to calculate [*P*], *i.e.*:

$$p_{ij}=\frac{1}{V_j\cdot V_i}\int_{V_i}\int_{V_j}\boldsymbol{G}\cdot\mathrm{d}v_j\cdot\mathrm{d}v_i \quad (14)$$

Now, the Green function becomes the only unknown. As long as we get ***G***, then the contact-to-contact capacitance (or admittance) will be easily calculated.

Here we only consider the case of both the point charge and the point of observation are in the same dielectric layer, on the surface with $z = z' = 0$. The Green function then changes to,

$$\boldsymbol{G}(x,y;x',y')_{z=z'=0}=(\boldsymbol{G}_0)_{z=z'=0}+\left(\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}f_{mn}C_{mn}\cos\left(\frac{m\cdot\pi\cdot x}{a}\right)\cos\left(\frac{m\cdot\pi\cdot x'}{a}\right)\cos\left(\frac{n\cdot\pi\cdot x}{b}\right)\cos\left(\frac{n\cdot\pi\cdot x'}{b}\right)\right) \quad (15)$$

where $C_{mn} = 0$ for ($m = n = 0$), $C_{mn} = 2$ for $m = 0$ or $n = 0$ but $m \neq n$ and $C_{mn} = 4$ for all others mn ($m > 0$) and ($n > 0$).

The function f_{mn} is given by:

$$f_{mn}=\frac{1}{ab\gamma\varepsilon_N}\frac{\beta_N\tanh(\gamma_{mn}\mathrm{d})+\Gamma_N}{\beta_N+\Gamma_N\tanh(\gamma_{mn}\mathrm{d})} \quad (16)$$

where

$$\gamma_{mn}=\sqrt{\left(\frac{m\cdot\pi\cdot x}{a}\right)^2+\left(\frac{n\cdot\pi\cdot y}{b}\right)^2} \quad (17)$$

β_N and Γ_N can be computed recursively from:

$$\begin{bmatrix}\beta_k\\\Gamma_k\end{bmatrix}=\frac{1}{2}\cdot\begin{bmatrix}1+\frac{\varepsilon_{k-1}}{\varepsilon_k} & \left(1-\frac{\varepsilon_{k-1}}{\varepsilon_k}\right)e^{2\theta_k}\\\left(1-\frac{\varepsilon_{k-1}}{\varepsilon_k}\right)e^{-2\theta_k} & 1+\frac{\varepsilon_{k-1}}{\varepsilon_k}\end{bmatrix}\begin{bmatrix}\beta_{k-1}\\\Gamma_{k-1}\end{bmatrix} \quad (18)$$

where $\theta_k=\gamma_{mn}(\mathrm{d}-\mathrm{d}_k)$, $\beta_0=1$, $\Gamma_0=-1$.

Substituting by the Green function and considering two rectangular contacts *i* and *j* whom the geometric data are given by x_1, x_2, y_1, y_2 and x_3, x_4, y_3, y_4.

The "coefficient-of-potential" matrix is calculated with the following equation, giving the potential of contact *i*, induced by an elementary charge spread all over the contact:

$$p_{ij}=\frac{\Gamma_N}{a\cdot b\cdot\varepsilon_N\cdot\beta_N}+\left\{\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}f_{mn}\cdot C_{mn}\cdot\frac{a^2\cdot b^2}{m^2\cdot n^2\cdot\pi^4}\cdot\frac{\left(\sin\left(m\cdot\pi\cdot\frac{x_2}{a}\right)-\sin\left(m\cdot\pi\cdot\frac{x_1}{a}\right)\right)\cdot\left(\sin\left(m\cdot\pi\cdot\frac{x_4}{a}\right)-\sin\left(m\cdot\pi\cdot\frac{x_3}{a}\right)\right)}{(x_2-x_1)\cdot(x_4-x_3)}\right.$$
$$\left.\times\frac{\left(\sin\left(n\cdot\pi\cdot\frac{y_2}{b}\right)-\sin\left(n\cdot\pi\cdot\frac{y_1}{b}\right)\right)\cdot\left(\sin\left(n\cdot\pi\cdot\frac{y_4}{b}\right)-\sin\left(n\cdot\pi\cdot\frac{y_3}{b}\right)\right)}{(y_2-y_1)\cdot(y_4-y_3)}\right\} \quad (19)$$

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And then we invert [P] to generate [$\boldsymbol{C}$] and extract contact-to-contact parasitic.

In practice, we adjoin a new calculation grid to the initial one (of a M·N dimension), in such a way that we can apply directly a discrete cosine transform (DCT) to accelerate the algorithm resolution.

To calculate the substrate resistance, the Green's method is formally equivalent. We have only to replace ε by $1/\sigma$ (= ρ) in the former analytical expressions and to consider the admittance matrix [$\boldsymbol{G}$] replacing the capacitance matrix [$\boldsymbol{C}$] to determine the different substrate resistances. A current spreading along all the contact is then consider instead of a Q (charge).

For instance, stating from some region of interest of the 0.35 μm CMOS technology cited above, first we approximate the actual profile by uniformly doped stacked layers.

3.2. Transmission Line Analogy for Multilayered Media

In its simplest form, a transmission Line (TL) is a pair of conductors linking together two electrical systems (source and load, for instance), with a forward (f) and return (r) paths; for cases where the return path (and the forward) is floating, a third conductor (or more) is introduced as the grounding shield. For microwaves, they are waveguides. In our case, the propagation of EM waves, their interferences, through the silicon substrate, is among the most serious obstacles in the steady trend towards integration of present day microelectronics. In fact the TL method (TLM) is well established; it can be seen as a more physical interpretation of the mathematical developments presented above, but equivalent.

The principal strength of this method is it is well dedicated to embedded contacts, in any number; for instance in **Figure 7(b)**, keeping the same location of the contacts in the < x, y > plane, we have been changing ad libitum their zi and zj contact altitudes. In practice, a region of interest of the 0.35 μm process is selected, and decomposed in twelve layers (see **Figure 8** and **Table 2**).

Let us consider a plane wave, which its plane of incidence parallel to the <z', z> plane; the medium it is incident upon is multilayered.

Then, we consider the general case in which the line's impedance is not the same as that of the load. Wave front A hits the load Z_L: a part of its energy is absorbed by Z_L, the remaining energy is reflected; in this case, voltage and current wave-fronts are not in phase. This reflected wave can meet another incident wave form B.

The direction of current flow depends on the polarity of the waveform at the time of observation; if two positive directed waveforms (one forward an one reflected) meet, the current waveforms subtract but the voltage

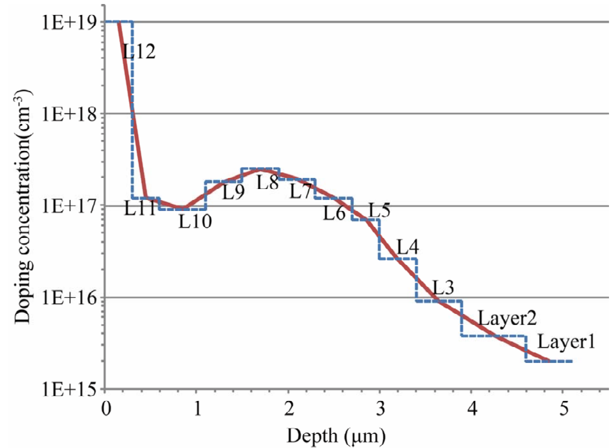

Figure 8. A specific depth profile of the 0.35 μm technology (p-region).

Table 2. Schematic doping profile values in the default p-region of the standard BiCMOS process.

Layer	Thickness (μm)	Concentration (cm^{-3})	Resistivity (Ω·m)	Conductivity (S/m)
12	0.3	1.00E+19	8.80963472E–05	11351.21
11	0.3	1.20E+17	1.70903883E–03	585.12
10	0.5	9.00E+16	2.13546702E–03	468.28
9	0.4	1.80E+17	1.26525401E–03	790.36
8	0.4	2.50E+17	1.00280455E–03	997.20
7	0.4	1.90E+17	1.21694516E–03	821.73
6	0.4	1.20E+17	1.70903883E–03	585.12
5	0.3	7.00E+16	2.61060351E–03	383.05
4	0.4	2.60E+ 16	6.06685659E–03	164.83
3	0.5	9.00E+15	1.60533251E–02	62.29
2	0.7	3.80E+15	3.65908063E–02	27.33
1	0.5	2.00E+15	6.83455581E–02	14.63

waveforms add. Likewise, if a positive directed waveform meets a negative directed waveform, the current will add and the voltage will subtract (**Figure 9**).

The expression for the apparent impedance is given below:

$$Z = \frac{V_{\text{total}}}{i_{\text{total}}} = \frac{V_f \pm V_r}{i_f \pm i_r} \tag{20}$$

staring for the general solution for voltages and currents:

$$V(z) = V_f e^{\gamma z} + V_r e^{-\gamma z} \tag{21}$$

$$I(z) = Y_c \left(V_f e^{-\gamma z} - V_r e^{\gamma z} \right) \tag{22}$$

where the propagation coefficient is the square root of Z

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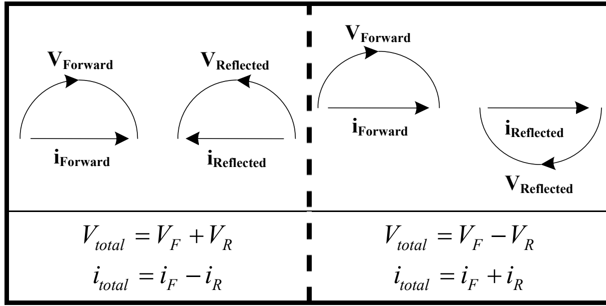

Figure 9. Two possible interactions between the voltage (current) of the forward wave and the voltage (current) of the reflected wave.

and Y product, respectively the linear impedance and admittance;

The $\gamma = \alpha + j\beta$; α attenuation, β = 360°/λ_{si} are derived directly from the chain matrix:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cosh\gamma L & Z_c \sinh\gamma L \\ Y_c \sinh\gamma L & \cosh\gamma L \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (23)$$

and from the output branch: $V_2 = -Z_L I_2$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = -I_2 \begin{bmatrix} Z_L \cosh\gamma L & Z_c \sinh\gamma L \\ Z_L Y_c \sinh\gamma L & \cosh\gamma L \end{bmatrix} \quad (24)$$

where $Z_c = 1/Y_c$ (square root of Z and Y ratio) is the characteristics impedance (Electric and magnetic fields modulus ratio), Z_L is the charge impedance, L is the distance from the load. We can extract an input impedance, said Z_l (= V_1/I_1), function of the load impedance Z_{l+1} (l: layer number) as:

$$Z_l = Z_c \frac{Z_{l+1} + Z_c \tanh\gamma L}{Z_c + Z_{l+1} \tanh\gamma L} \quad (25)$$

This very well known (TLM) equation Z_l is directly related to Equation (16).

In fact, restarting from Equation (12), taking into account the limit or boundary conditions—continuity of potential, and the discontinuity of the electric field if there is a surface charge at the considered layer interface—it is quite easy to program this iterative solution (versus substrate depth, or layers) of Equation (12).

Regarding the injected current source point (contact), there are two classes of layers, upper (up) and lower (lo) ones. Then we introduce in our program [11] the derivation current (for instance, in the upper layer):

$$I = \frac{Z_{up}}{Z_{up} + Z_{lo}} V \quad (26)$$

In our simulator, we use a matricial formalism, extending the impedance and the current transmission from a layer l to its adjacent (cf. Equation (16) or Equation (25)), starting from a k layer:

$$\begin{bmatrix} Z_{k,l+1} \\ T_{k,l+1} \end{bmatrix} = \begin{bmatrix} A_k & -B_k \\ C_k & -D_k \end{bmatrix} \begin{bmatrix} Z_{k,l} \\ T_{k,l} \end{bmatrix} \quad (27)$$

4. First Green/TLM Results

First of all, we did some numerical experiences using COMSOL® [6], a well known multiphysics (cf. thermal, mechanical couplings) simulator; it is also a dedicated tool for full wave electromagnetic analysis. It uses essentially Galerkin-like algorithms. Typically a 3D simulation can use a few ten of minutes or hours.

For instance, we compare it, with a very good accuracy, with the analytical formula associated to an "R//C" filter (see, for instance: **Figure 10**; Resistivity bulk: 10 Ω·cm, 2 contacts: 50 × 50 μm^2, distant of 200 μm); we obtain the following extracted parameters: R = 2.3 KΩ, C = 4.5 fF.

Now it is very easy to calculate, by TLM method any transfer impedance. Possibly embedded in the substrate, contacts can be introduced into any layer; they can be real (metal like) or virtual. Presented is a two contacts example on the **Figure 11**; the he surface die is 30 μm × 30 μm, with M = N = 300, surface contact: 20 points × 20 points (the calculation point, M·N, are equidistributed).

The Green function $G(z, z')$ describing the electric field response to the unity current is identifiable to the transfer impedance between any two points; then we can calculate this impedance spreading. We can extract the potential, particularly between two contacts. This way, we use the inverse transform of the Kroneker matricial product of the impedance by the current DCT. For instance, as a first check, we present on the **Figure 12** the impedance module for two in-depth contacts, at the interfaces: L_5/L_6 and L_9/L_{10}; the comparison between "TLM/Green" and "COMSOL" is quite good.

5. Conclusions

An efficient and elegant technique to model substrate coupling, via frequency dependant impedance extraction,

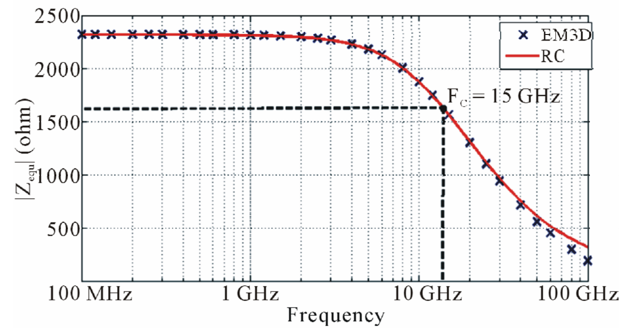

Figure 10. Impedance: comparison between COMSOL and the analytical result "R//C" (Resistivity bulk: 10 Ω·cm; 2 contacts: 50 × 50 μm^2, distant of 200 μm).

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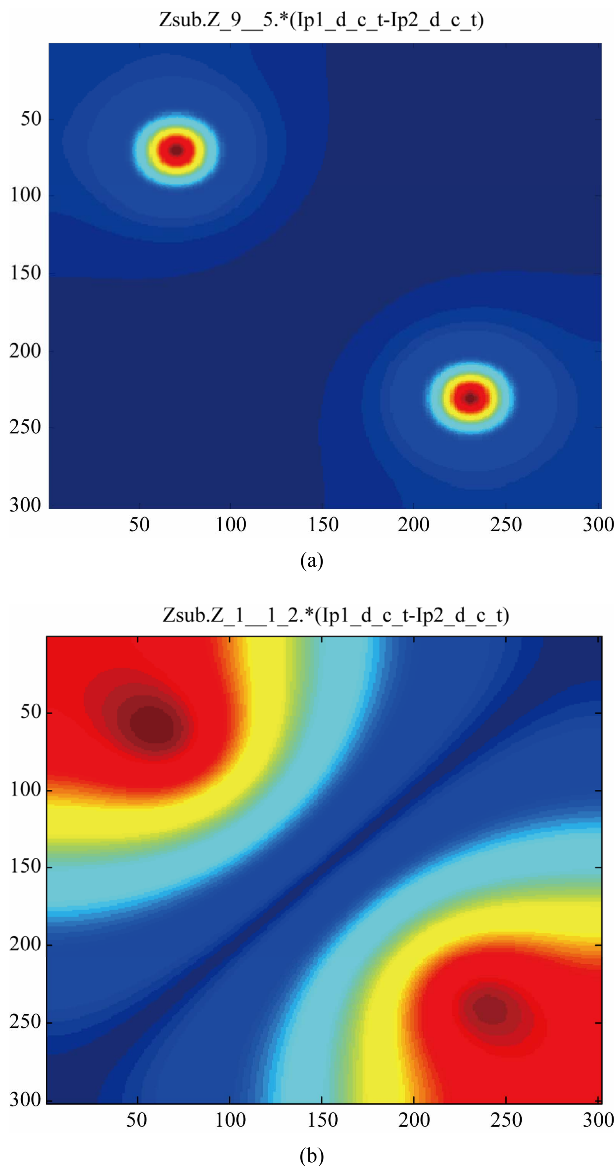

Figure 11. Potential distributions via transfer impedance (from red to dark blue: voltage decreasing). (a) Contacts embedded in the bulk; interfaces: L_5/L_6 and L_9/L_{10}; (b) Contacts at surface and bottom.

has been presented and programmed. The technique uses a combination of the classical Green function or transmission line method approach and the use of Fast Fourier Transform. The speed of this latter technique makes it suitable for optimization of circuit layout and for minimization of substrate coupling related effects. But the model is often limited to contact locations at the surface; in practice, in our work, the contacts can be placed anywhere in the substrate, so a new research should be enhanced in 3D.

For the near future, considering for instance our compatible 0.35 µm CMOS predilection technology, the digital part can attack any region from the substrate, the analogical CMOS or HBT devices, via a stochastic probability matrix derived from the switching activity [12]; the parasitic wave or impulsion aggressions can be derived via our transfer impedance methods; In fact, we could calculate a two point spectral density of current fluctuations, knowing that our method can handle any number of contacts. The ultimate goal will be to build a "whole" compact model dedicated to actual 3D circuits.

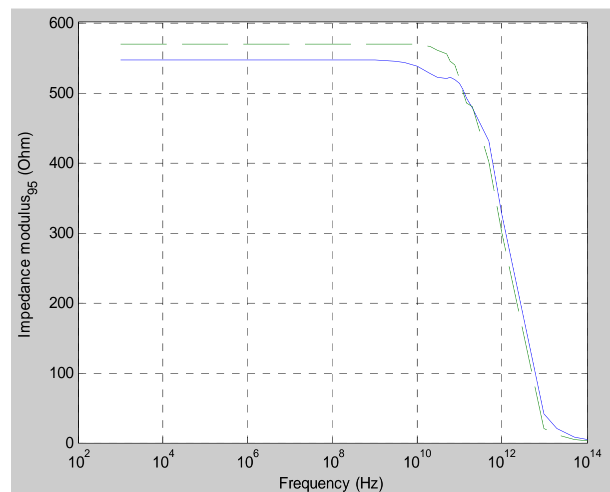

Figure 12. Comparison between finite element method (dashed-upper-line) and Green/TLM (solid-lower-line) (layer interfaces: L_5/L_6 and L_9/L_{10}).

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